Nanoscale III-V CMOS

J. A. del Alamo

Microsystems Technology Laboratories
Massachusetts Institute of Technology

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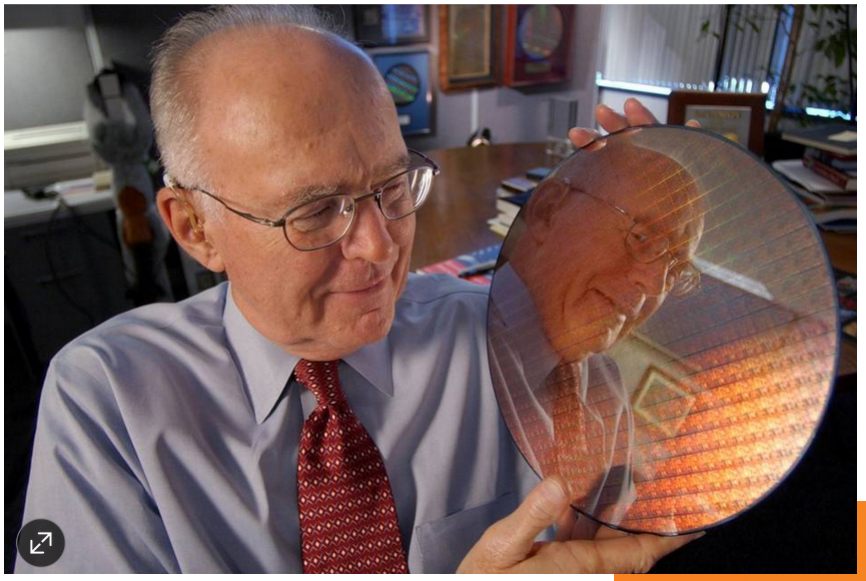
- Students and collaborators: D. Antoniadis, J. Lin, W. Lu, A. Vardi, X. Zhao
- Sponsors: Applied Materials, DTRA, KIST, Lam Research, Northrop Grumman, NSF, Samsung
- Labs at MIT: MTL, EBL

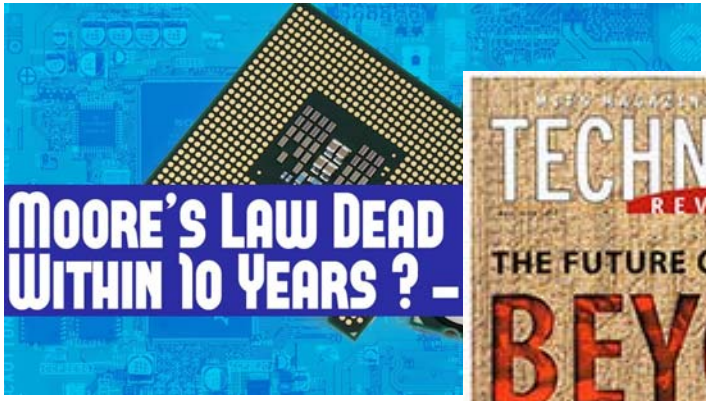
Moore's Law at 50: the end in sight?

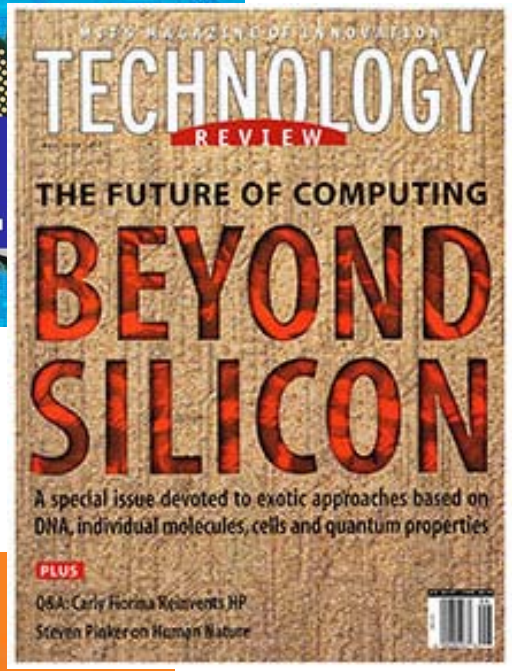
THE WALL STREET JOURNAL.

Moore's Law Is Showing Its Age

The prediction about squeezing transistors onto silicon has been revised again.

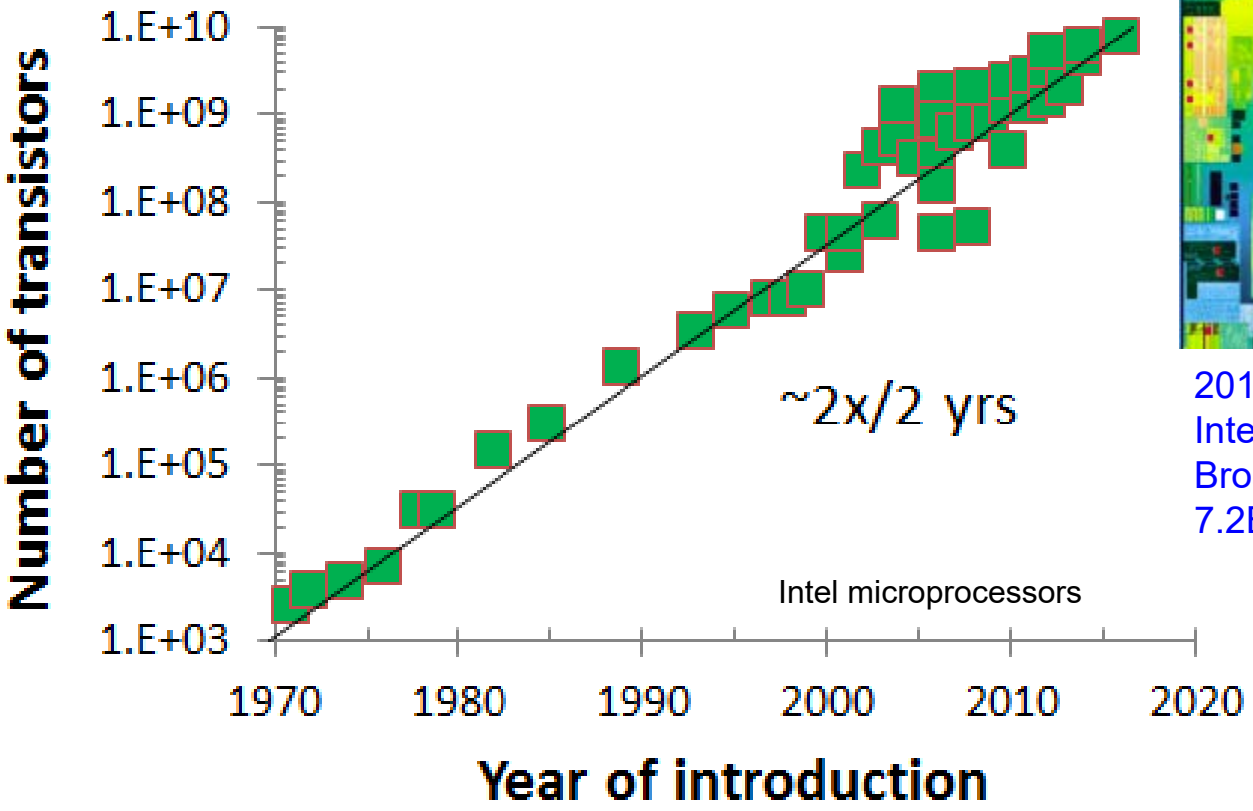


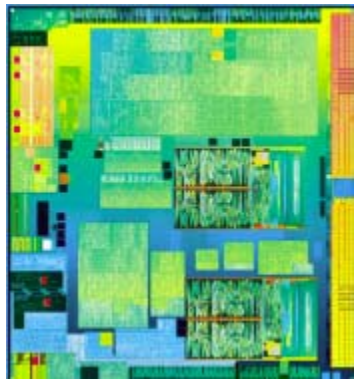




Moore's Law

Moore's Law = exponential increase in transistor density

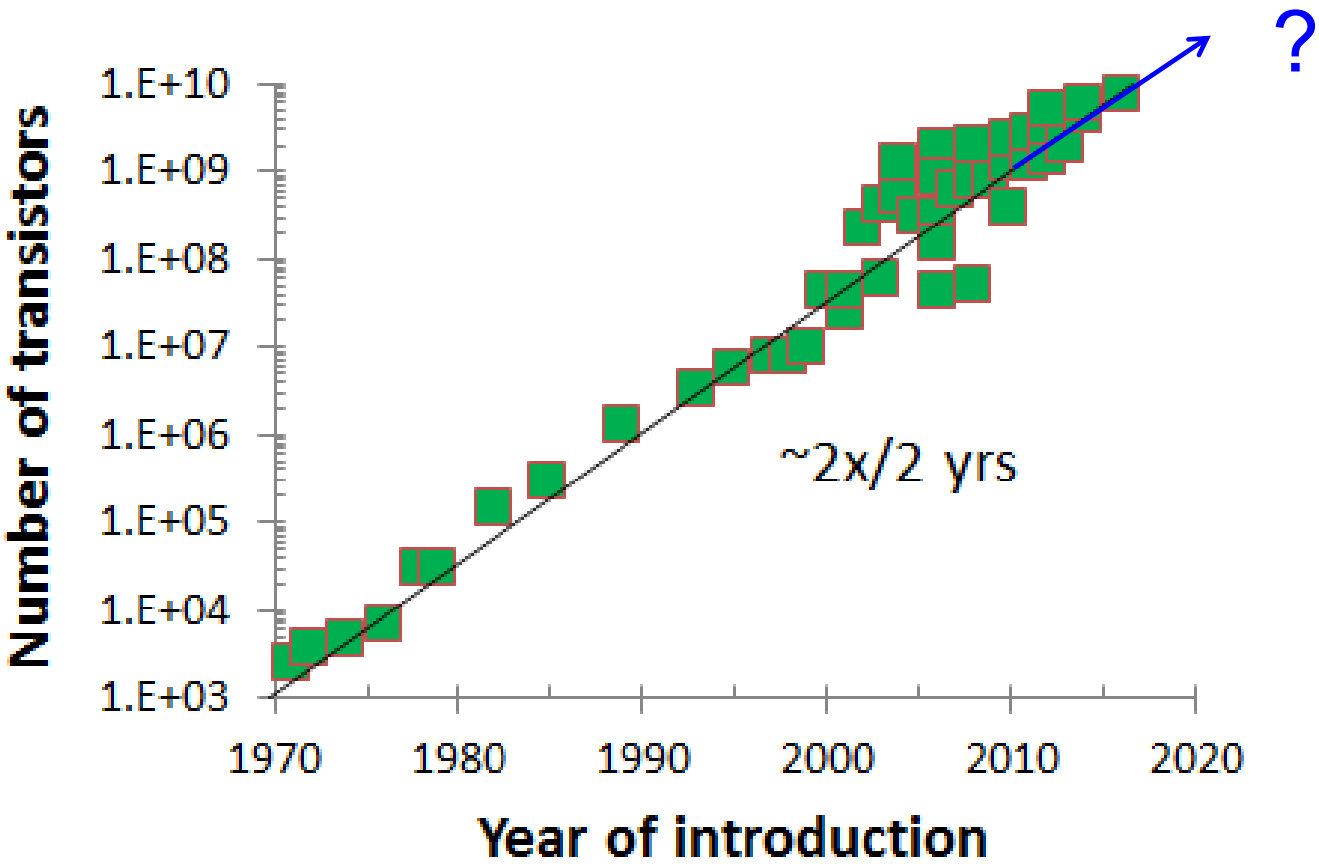




2016:
Intel 22-core Xeon
Broadwell-E5
7.2B transistors

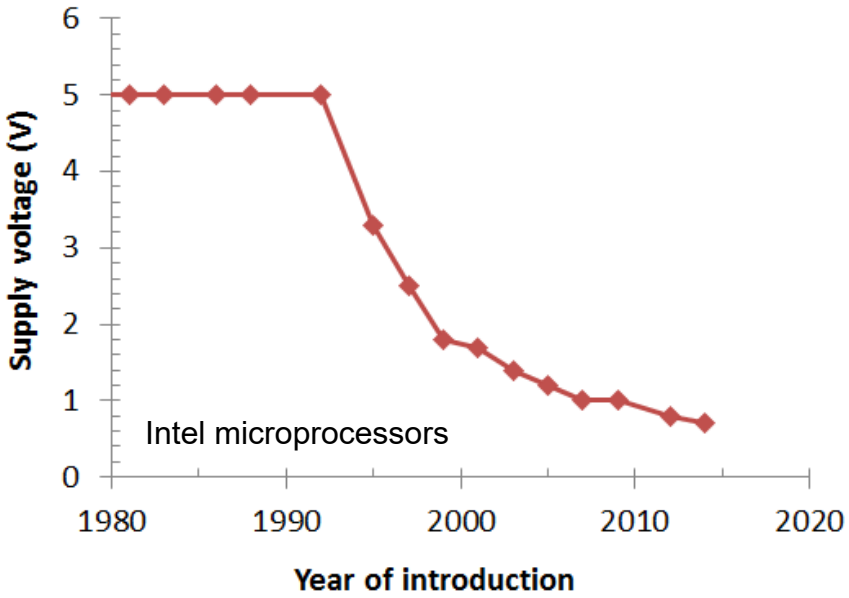
Moore's Law

How far can Si support Moore's Law?

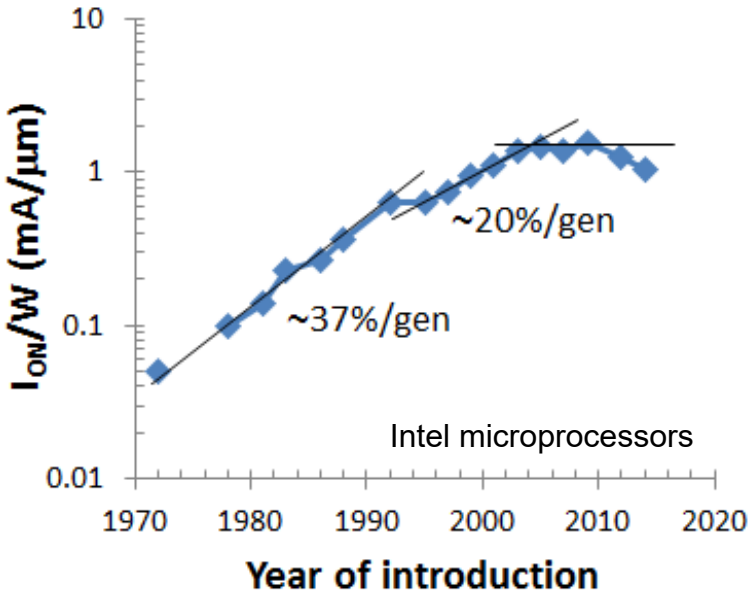


Transistor scaling → Voltage scaling → Performance suffers

Supply voltage:



Transistor current density:

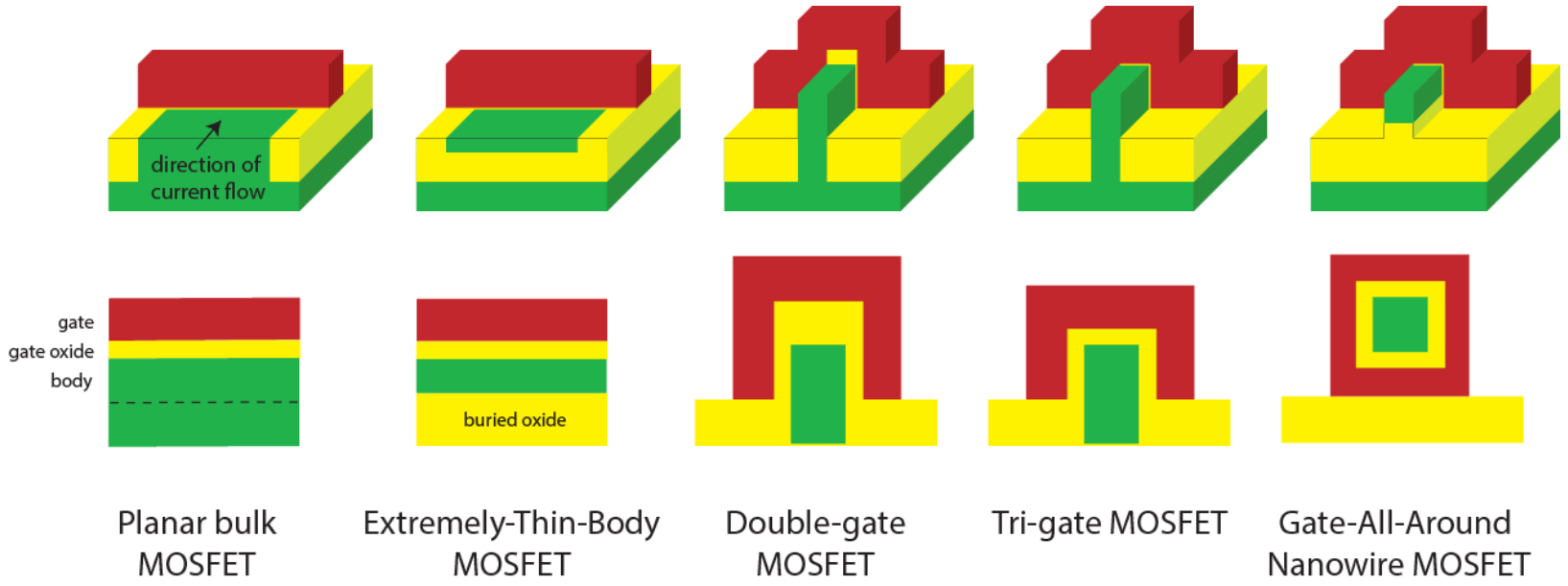


Goals:

- Reduced footprint with moderate short-channel effects
- High performance at low voltage

Moore's Law: it's all about MOSFET scaling

1. New device structures with improved scalability:

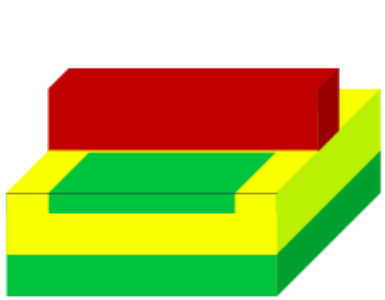


2. New materials with improved transport characteristics:

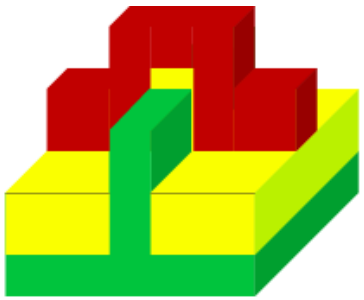
n-channel: Si → Strained Si → SiGe → InGaAs

p-channel: Si → Strained Si → SiGe → Ge → InGaSb

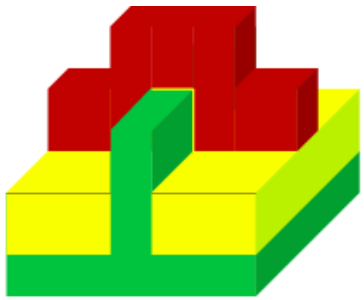
Contents

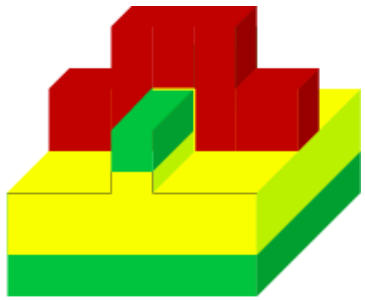


1. Planar InGaAs MOSFET

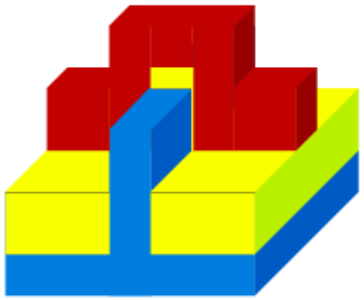


2. InGaAs FinFETs



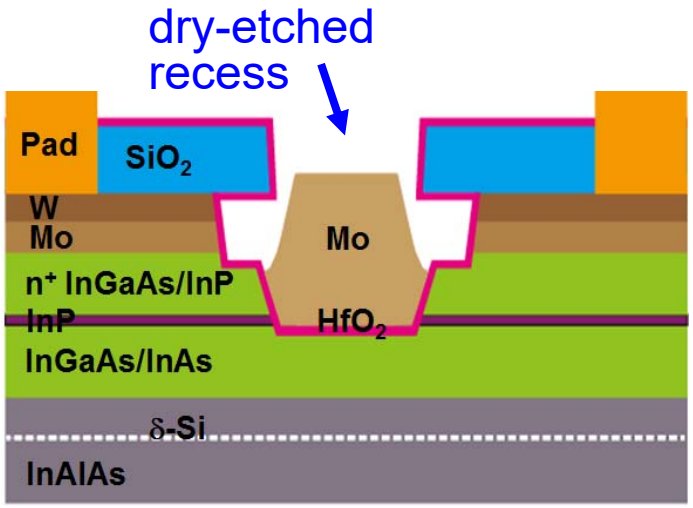


3. Gate-All-Around Nanowire MOSFET

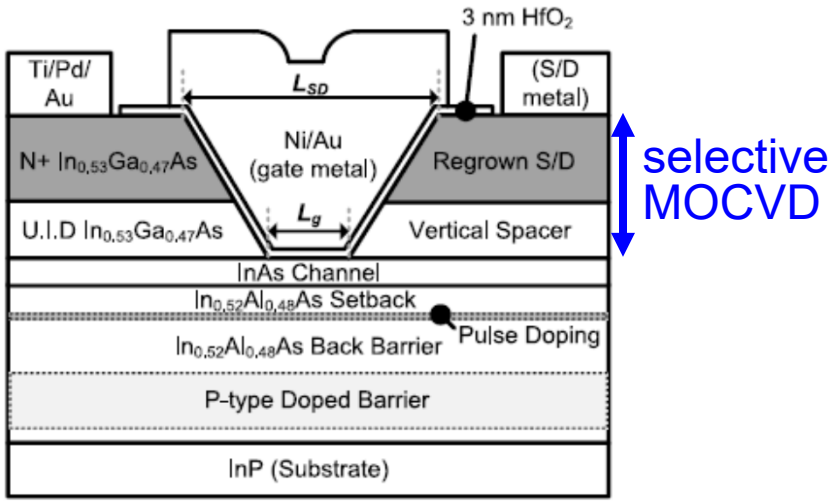


4. InGaSb FinFETs

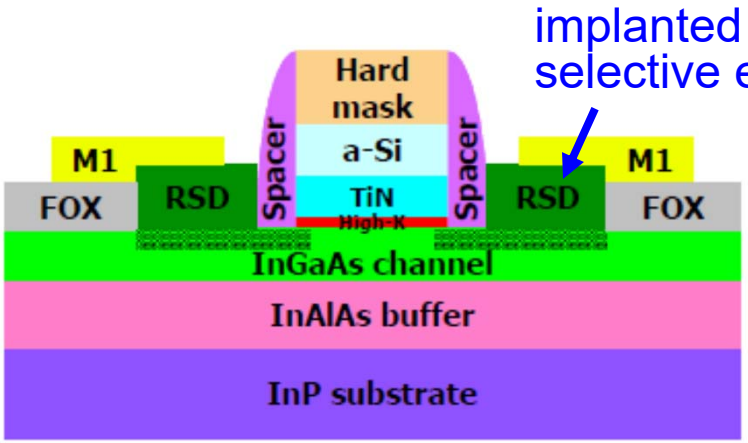
1. Self-aligned Planar InGaAs MOSFETs



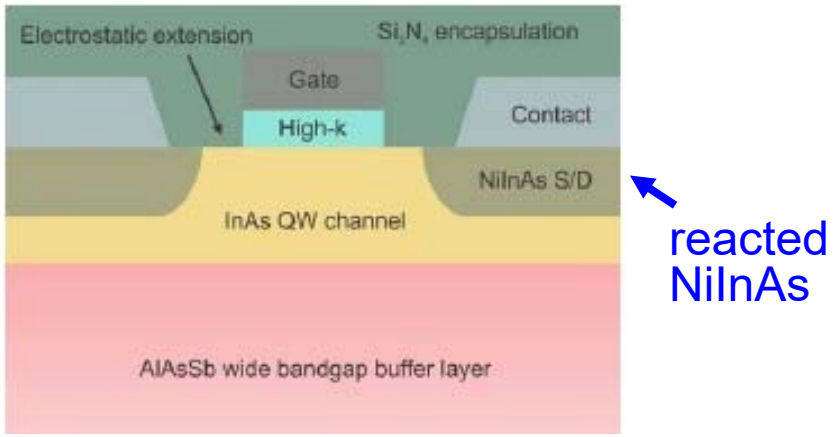
Lin, IEDM 2012, 2013, 2014



Lee, EDL 2014; Huang, IEDM 2014

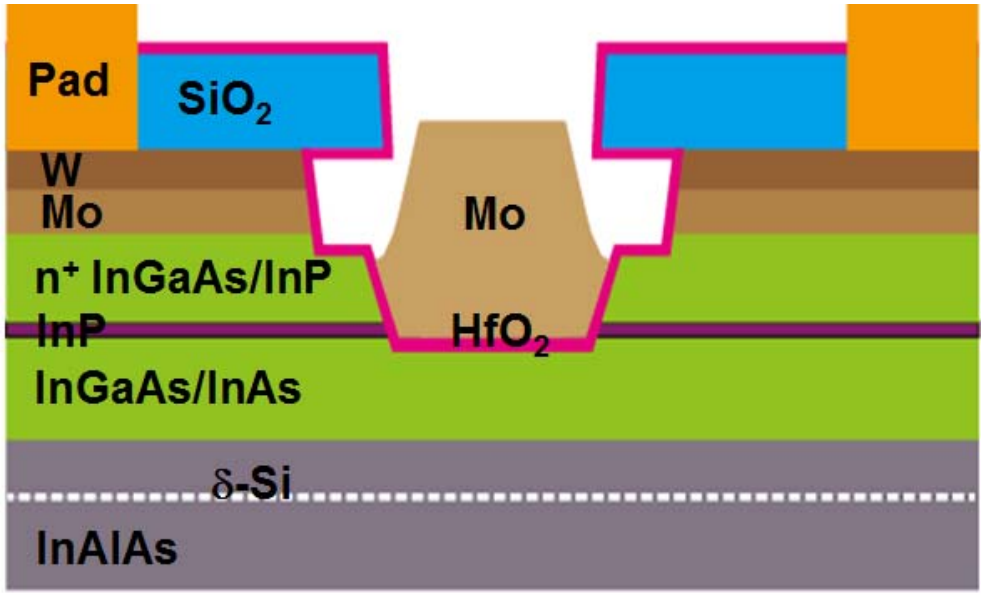


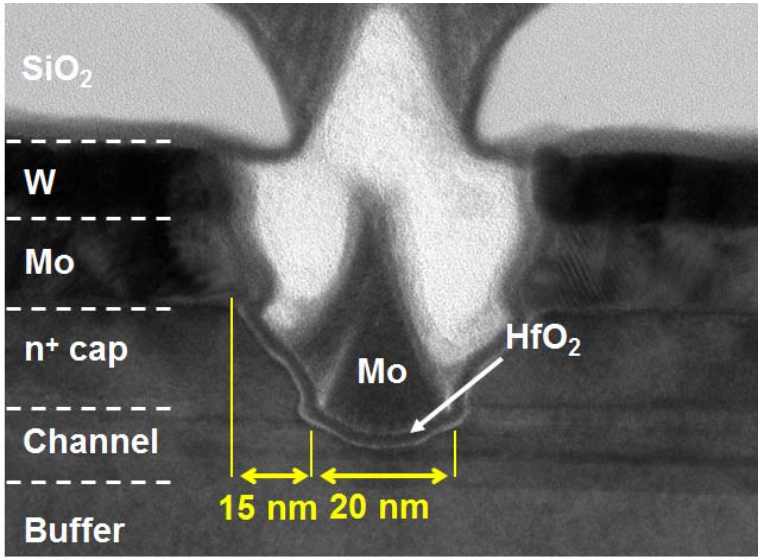
Sun, IEDM 2013, 2014



Chang, IEDM 2013

Self-aligned Planar InGaAs MOSFETs @ MIT

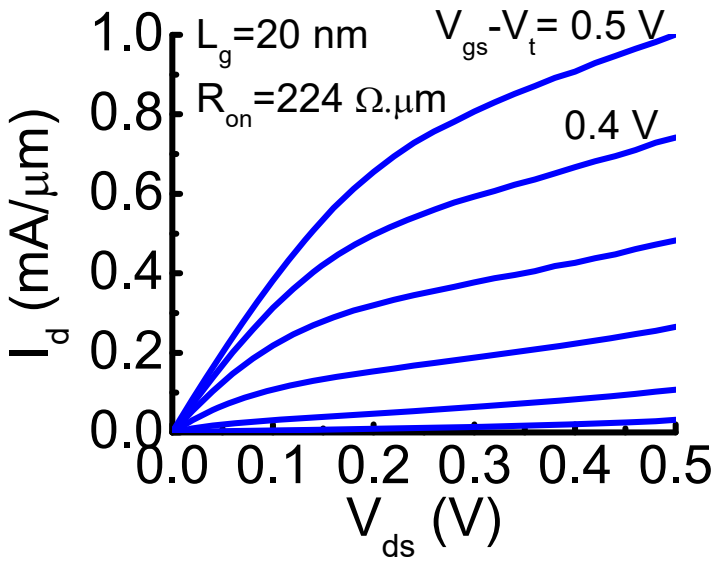




Lin, IEDM 2012, 2013, 2014

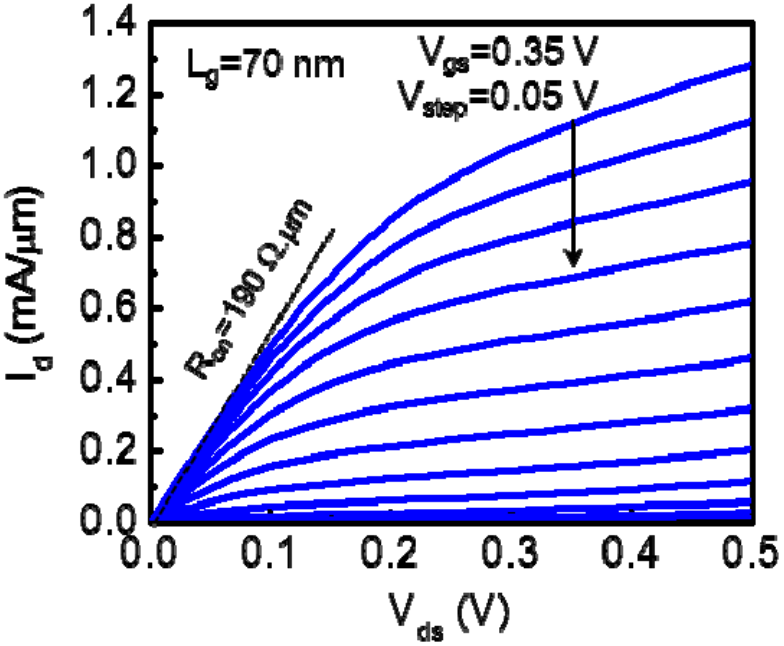
Recess-gate process:

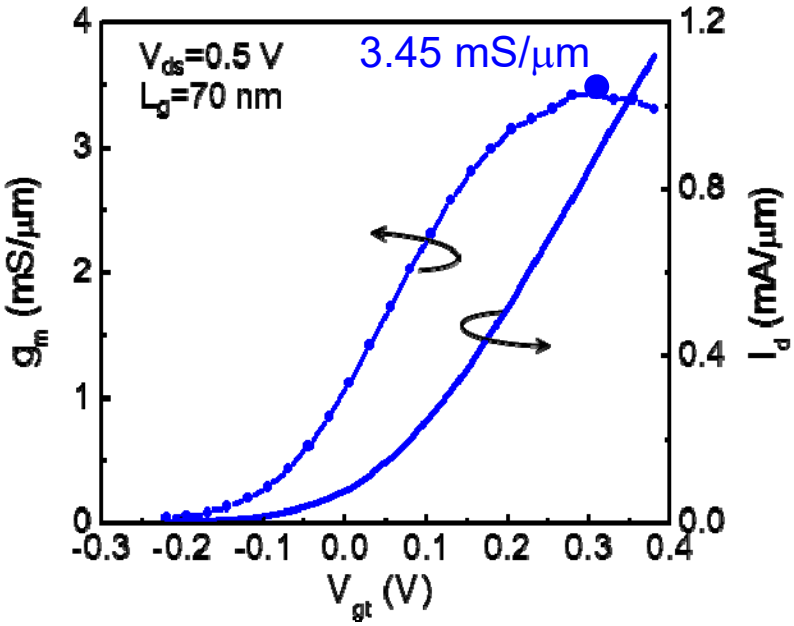
- CMOS-compatible
- Refractory ohmic contacts
- Extensive use of RIE



Highest performance InGaAs MOSFET

- Channel: $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$
- Gate oxide: HfO_2 (2.5 nm, EOT~ 0.5 nm)





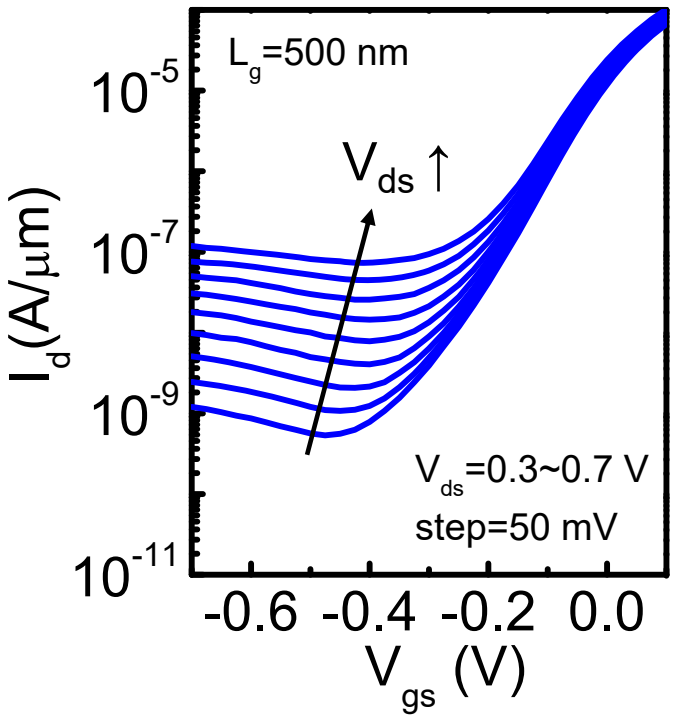
L_g=70 nm:

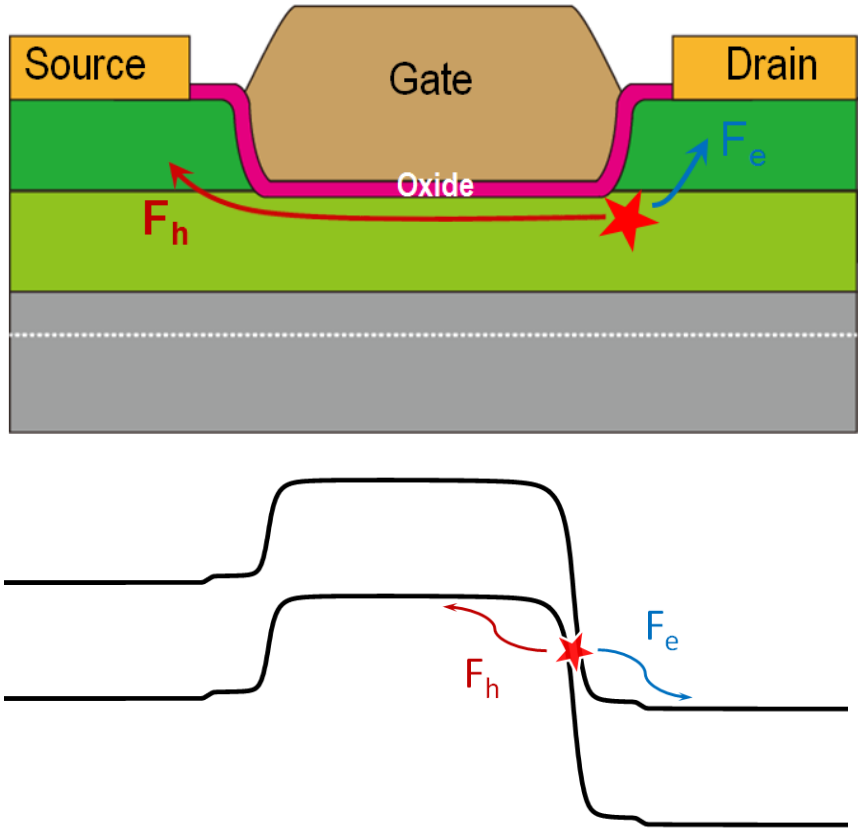
- Record $g_{m,max}$ = 3.45 mS/mm at V_{ds}= 0.5 V
- R_{on} = 190 Ω.mm

Lin, EDL 2016

Excess OFF-state current

Transistor fails to turn off:



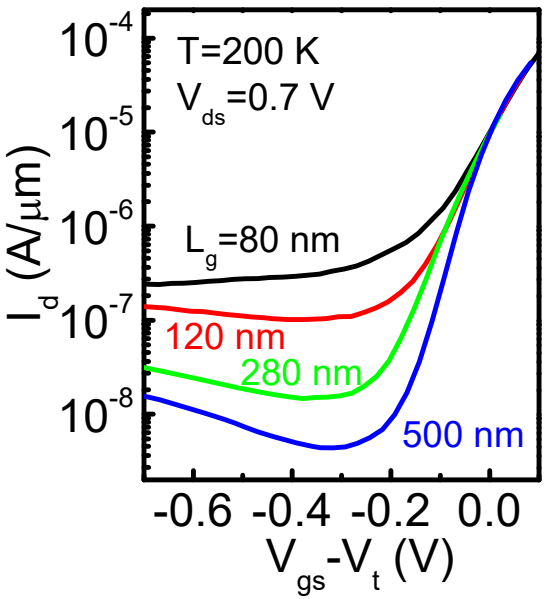


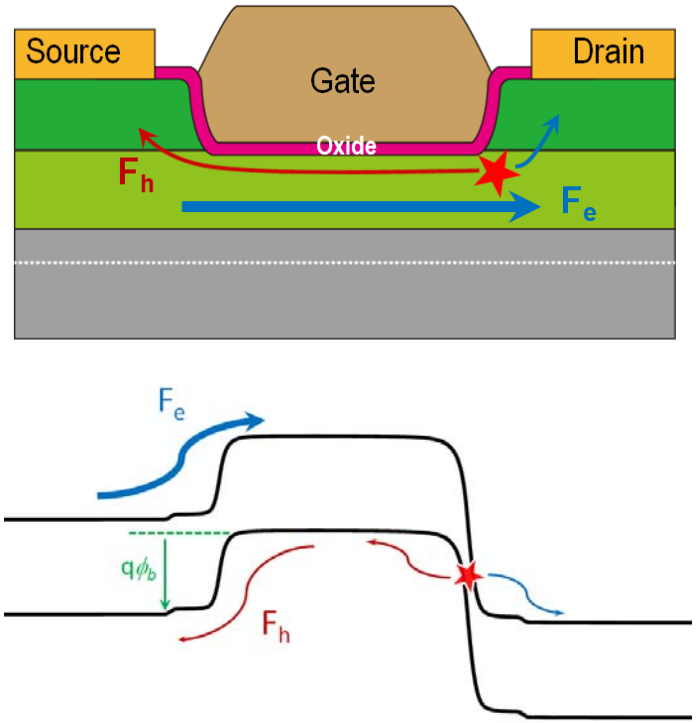
OFF-state current enhanced with V_{ds}

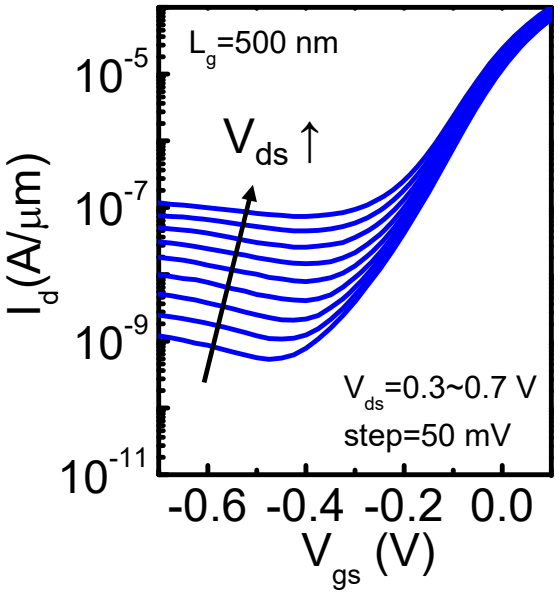
→ *Band-to-Band Tunneling (BTBT) or Gate-Induced Drain Leakage (GIDL)*

Lin, IEDM 2013

Excess OFF-state current



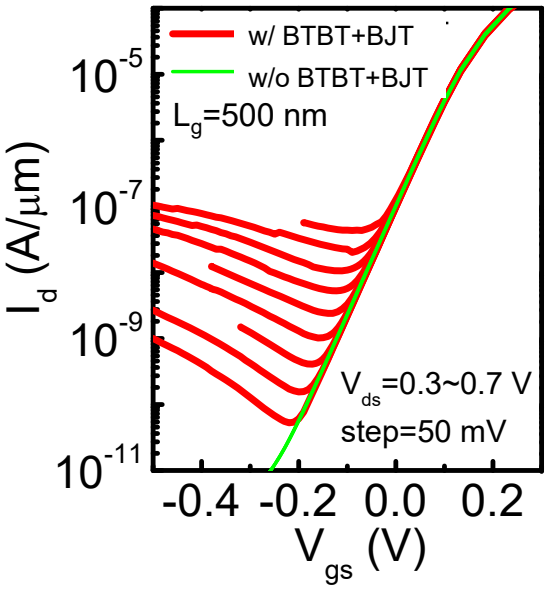




Lin, EDL 2014

Lin, TED 2015

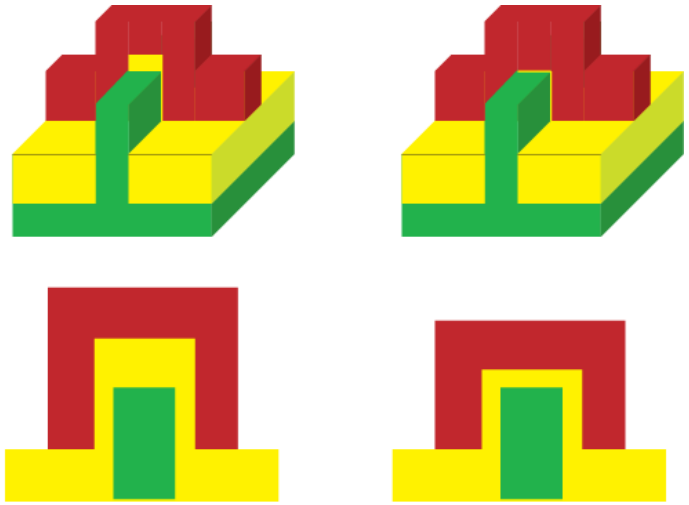
Simulations



L_g↓ → OFF-state current ↑

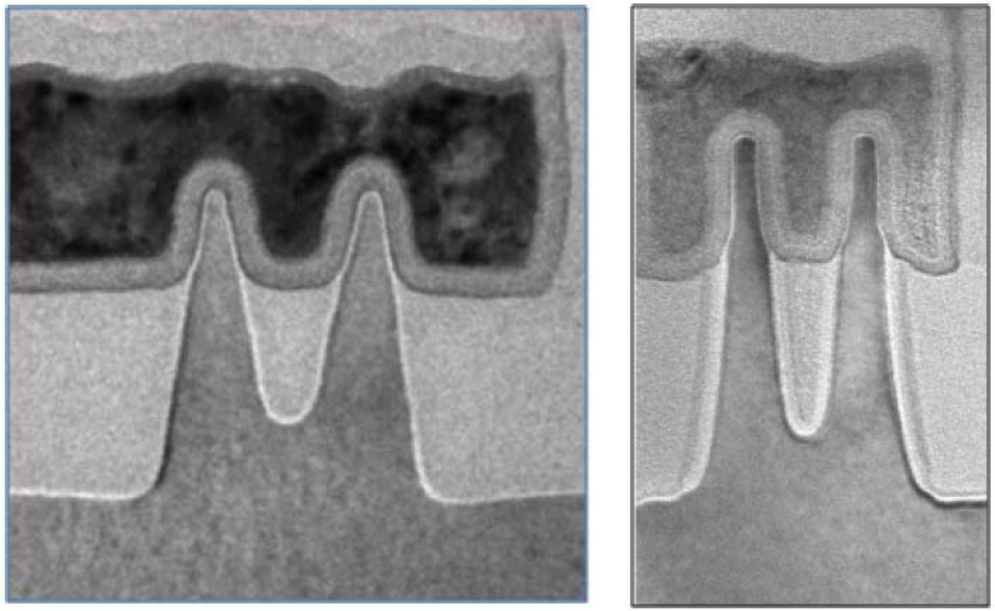
→ *bipolar gain effect due to floating body*

2. InGaAs FinFETs



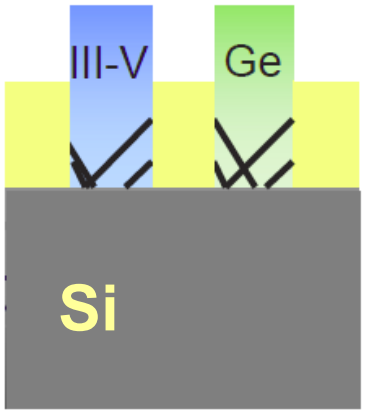
Double-gate MOSFET Tri-gate MOSFET

Intel Si Trigate MOSFETs

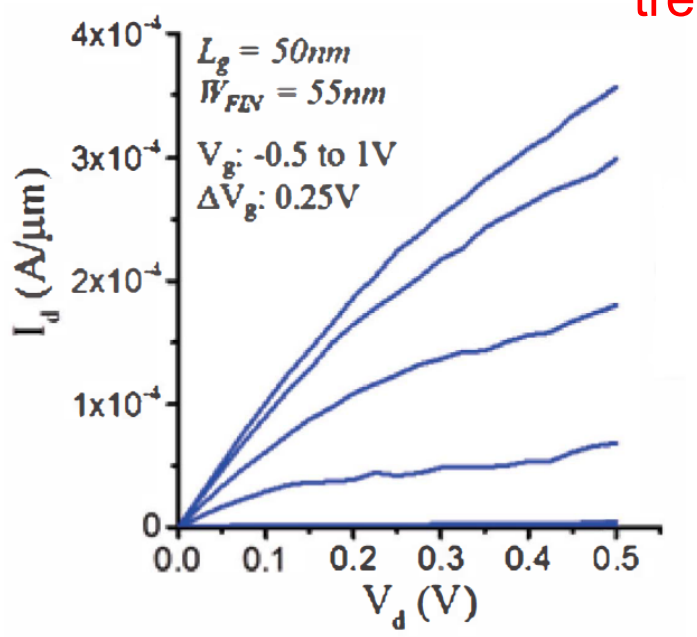


22 nm Process 14 nm Process

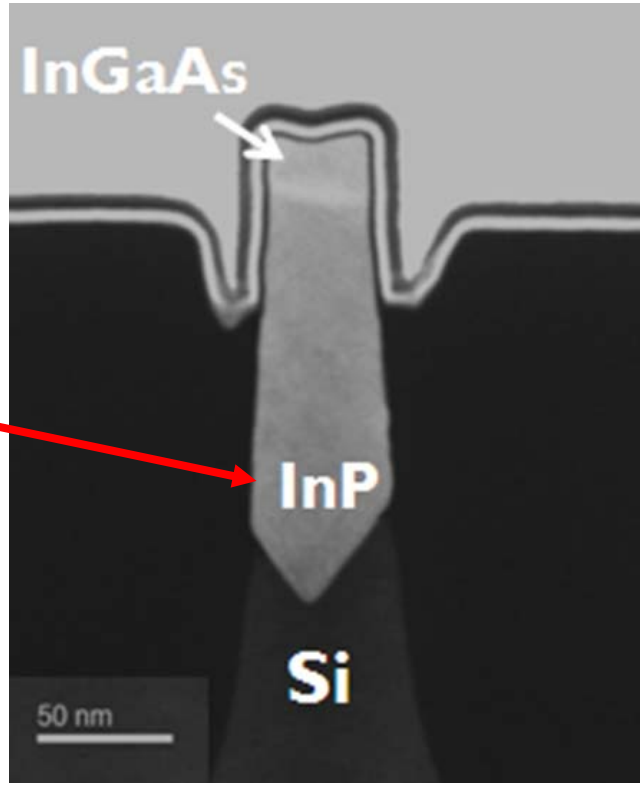
Bottom-up InGaAs FinFETs



Aspect-Ratio Trapping
Fiorenza, ECST 2010

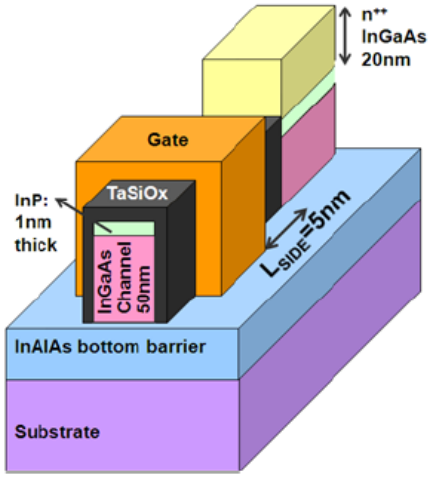


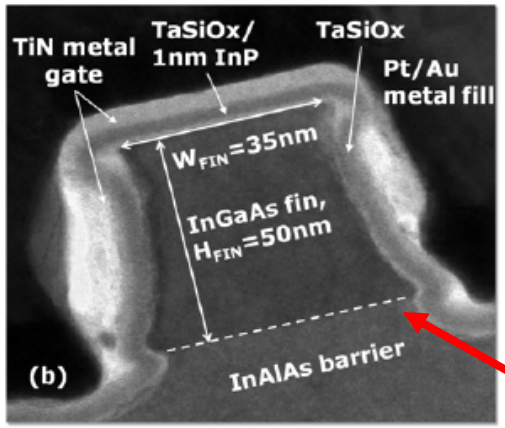
Epi-grown fin inside trench



Waldron, VLSI Tech 2014

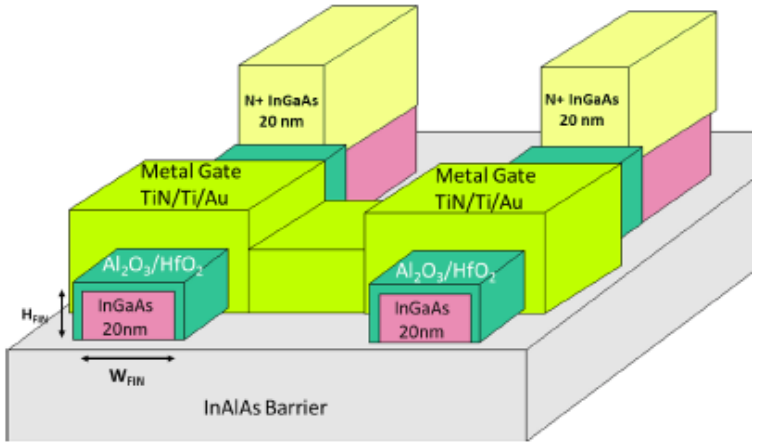
Top-down InGaAs FinFETs

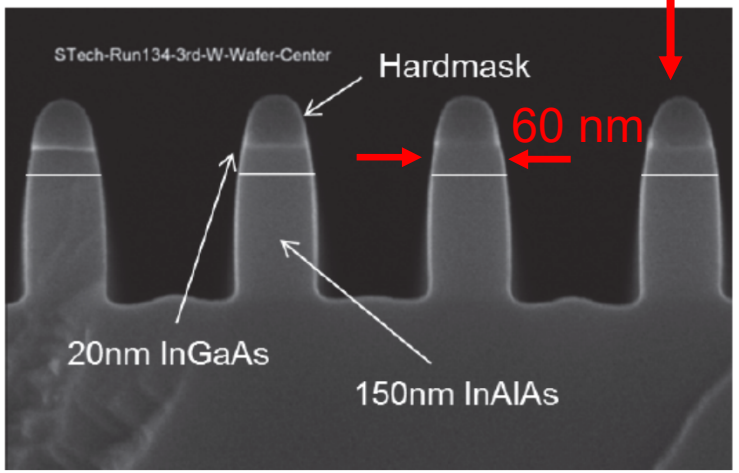




dry-etched fins

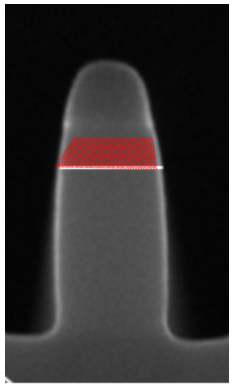
Radosavljevic, IEDM 2010

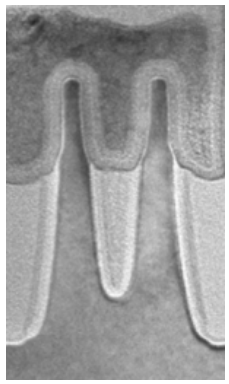




Kim, IEDM 2013

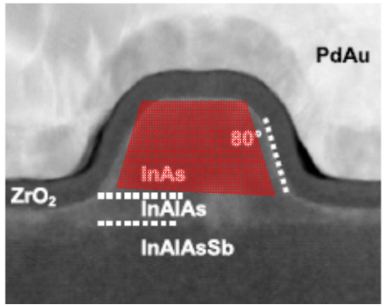
InGaAs FinFETs: g_m





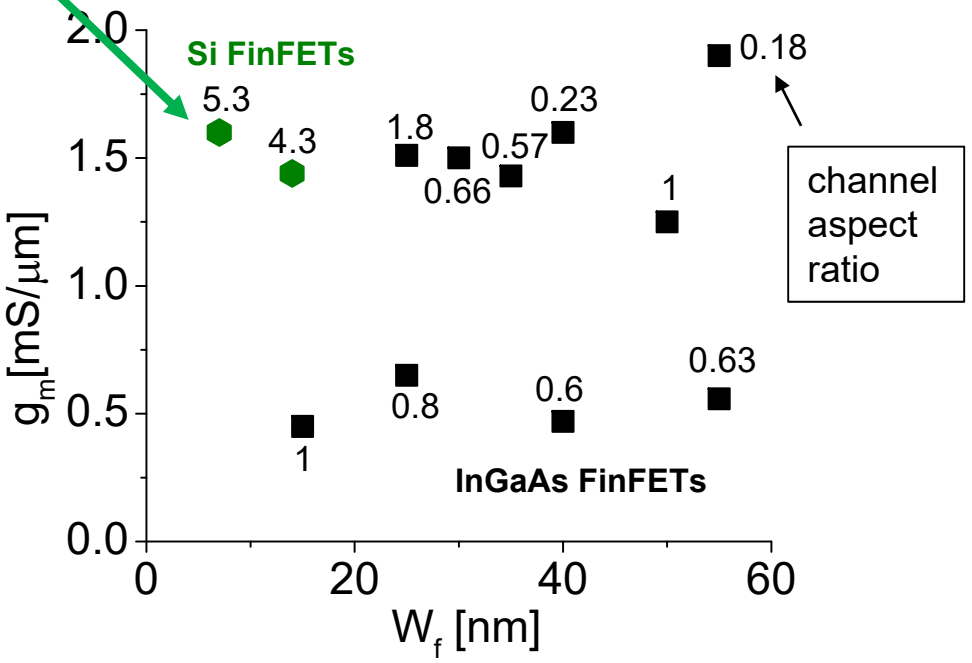
Natarajan, IEDM 2014

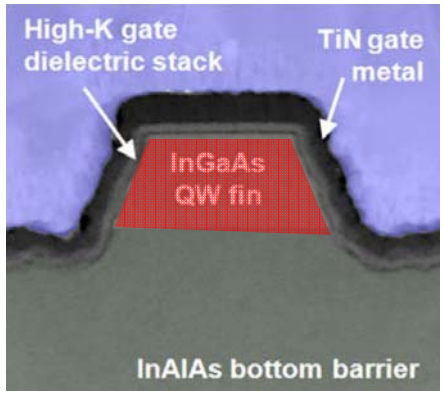
Kim, IEDM 2013



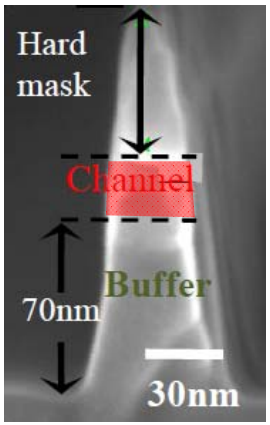
Oxland, EDL 2016

g_m normalized by width of gate periphery





Radosavljevic, IEDM 2011

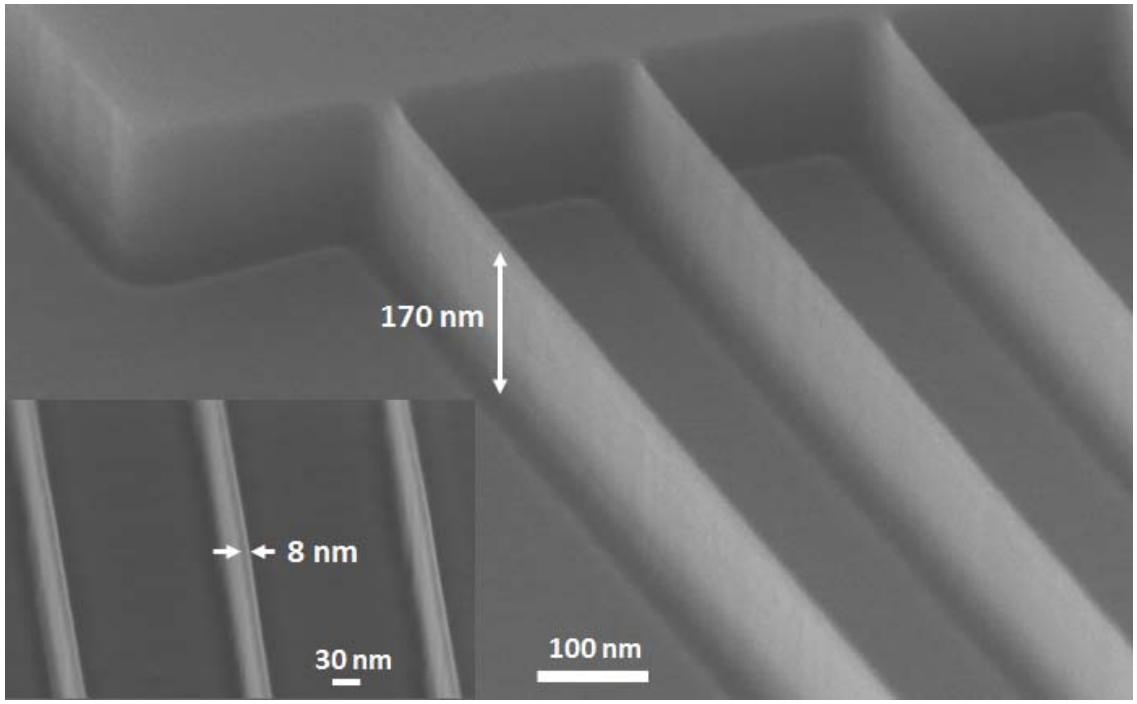


Thathachary, VLSI 2015

- Narrowest InGaAs FinFET fin: W_f=15 nm
- Best channel aspect ratio of InGaAs FinFET: 1.8
- g_m much lower than planar InGaAs MOSFETs

InGaAs FinFETs @ MIT

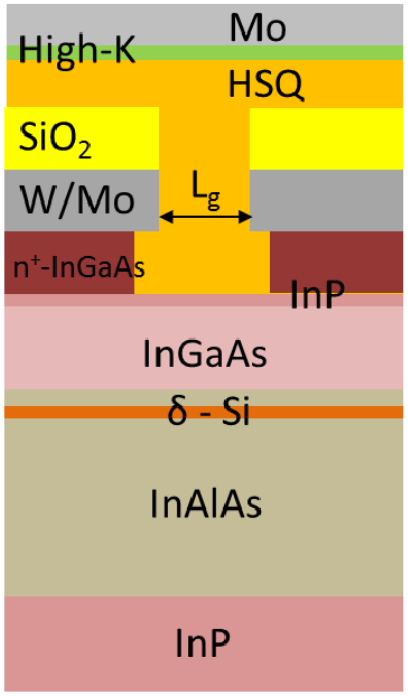
Key enabling technologies: $BCl_3/SiCl_4$/Ar RIE + digital etch

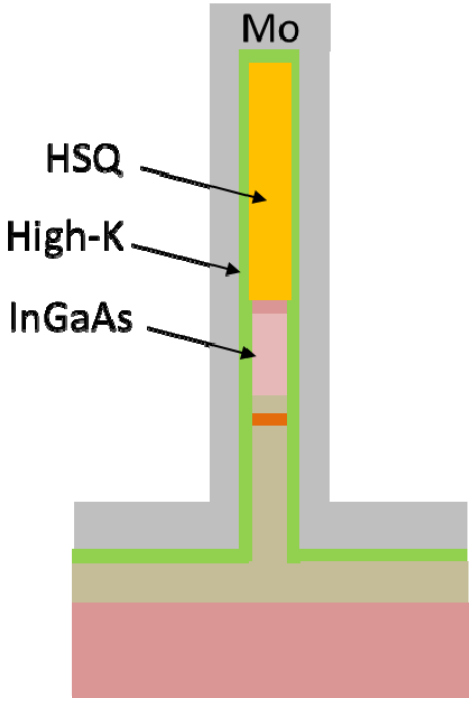


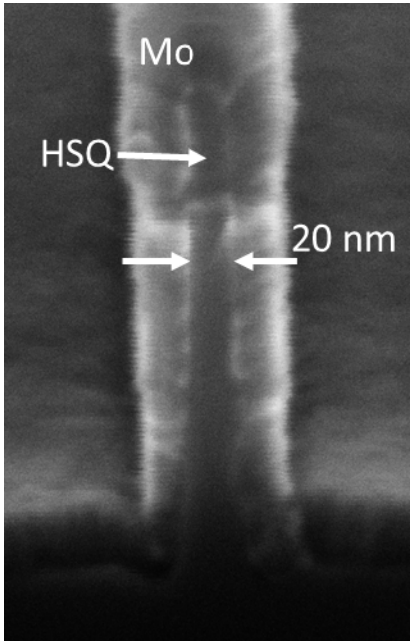
- Sub-10 nm fin width
- Aspect ratio > 20
- Vertical sidewalls

Vardi,
DRC 2014,
EDL 2015,
IEDM 2015

InGaAs FinFETs @ MIT





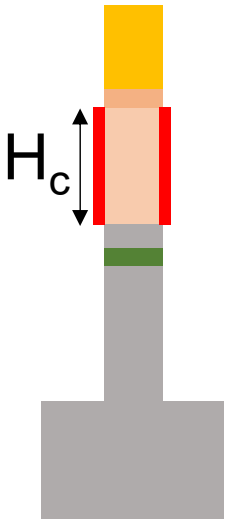


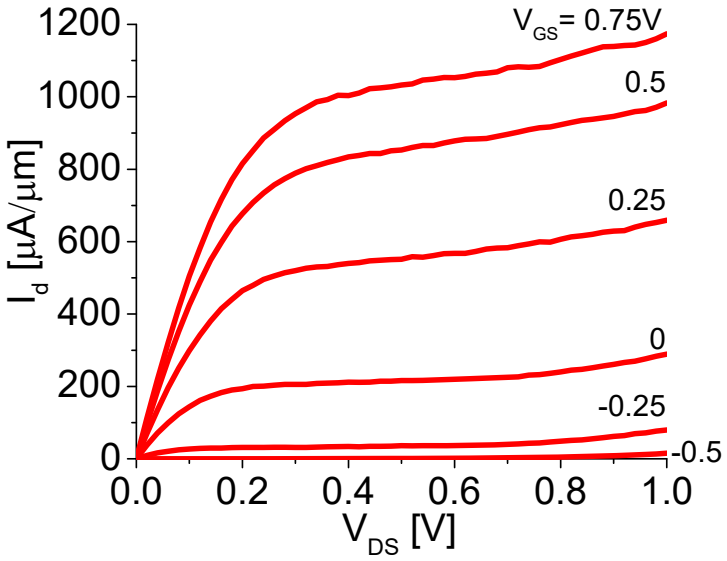
Vardi, VLSI Tech 2016

- CMOS compatible process
- Mo contact-first process
- Fin etch mask left in place → double-gate MOSFET

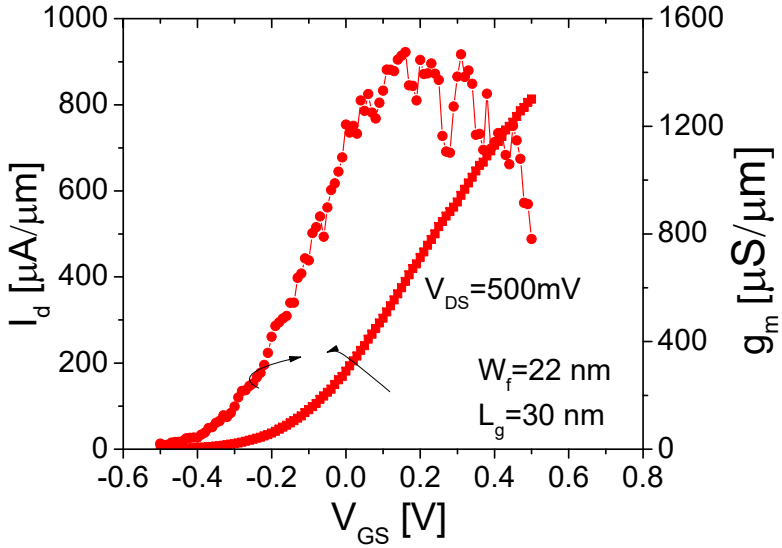
InGaAs FinFETs @ MIT

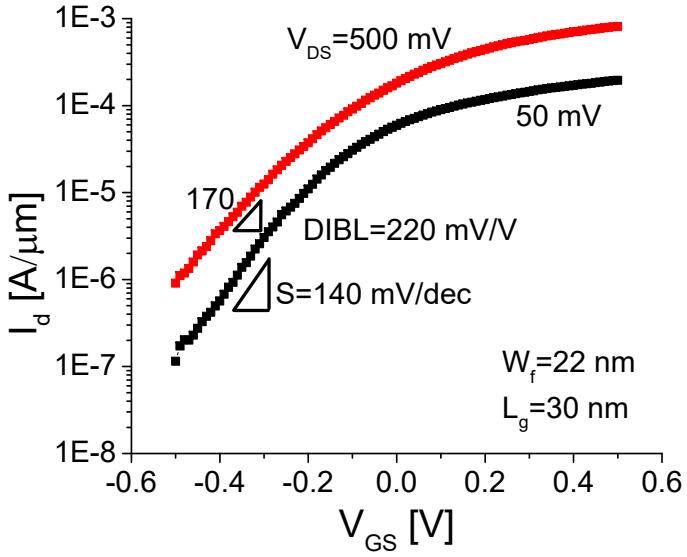
L_g=30 nm, W_f=22 nm, H_c=40 nm (AR=1.8):





Current normalized by 2xH_c





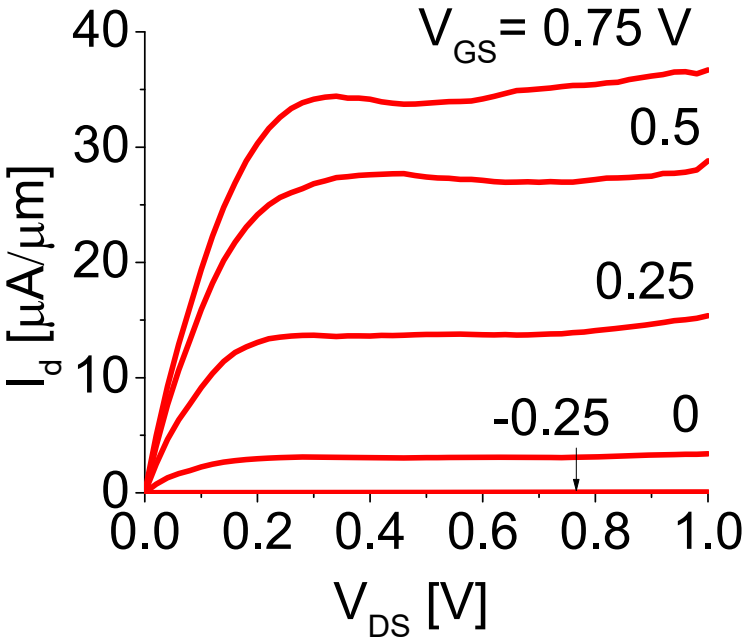
At V_{DS}=0.5 V:

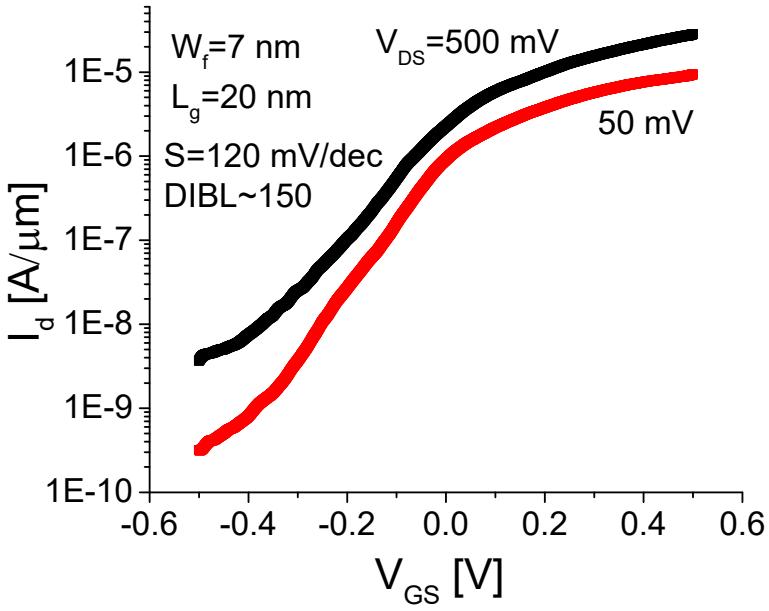
- g_m=1.4 mS/μm
- R_{on}=170 Ω.μm
- S_{sat}=170 mV/dec

Vardi, VLSI Tech 2016

Most aggressively scaled FinFET

L_g=20 nm, W_f=7 nm, H_c=40 nm (AR=5.7):





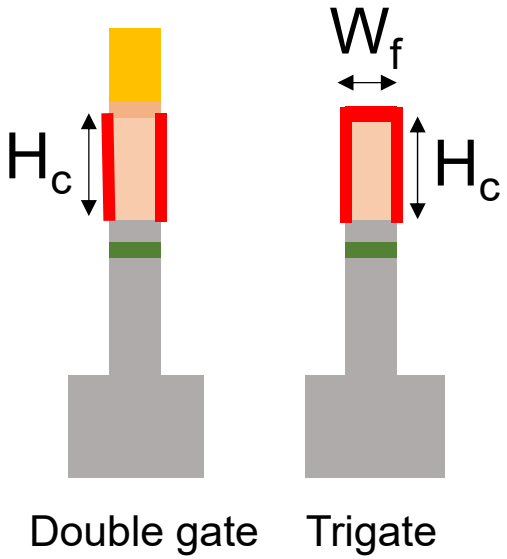
At V_{DS}=0.5 V:

- g_m=170 µS/µm
- R_{on}=4 kΩ.µm
- S_{sat}=130 mV/dec

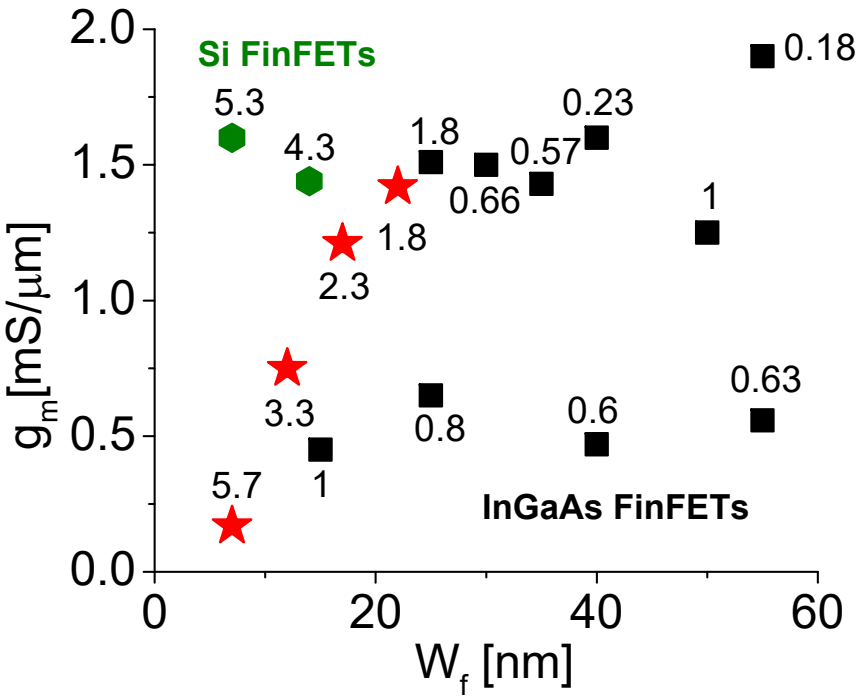
Vardi, VLSI Tech 2016

InGaAs FinFETs: g_m benchmarking

g_m normalized by width of gate periphery:



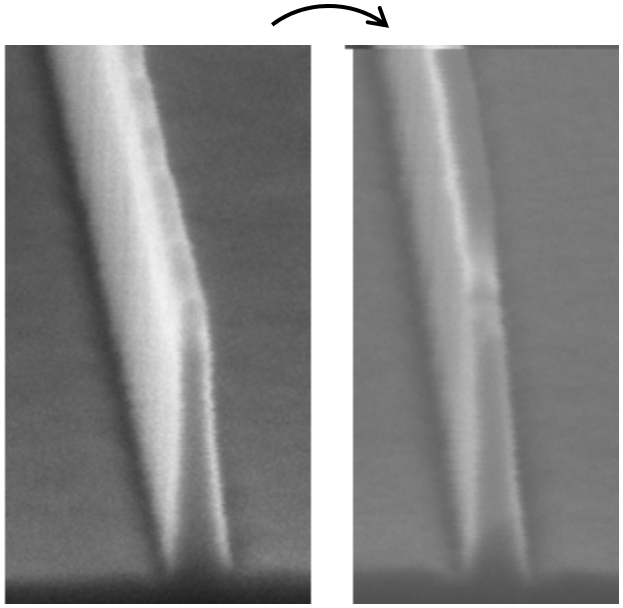
Vardi, VLSI Tech 2016



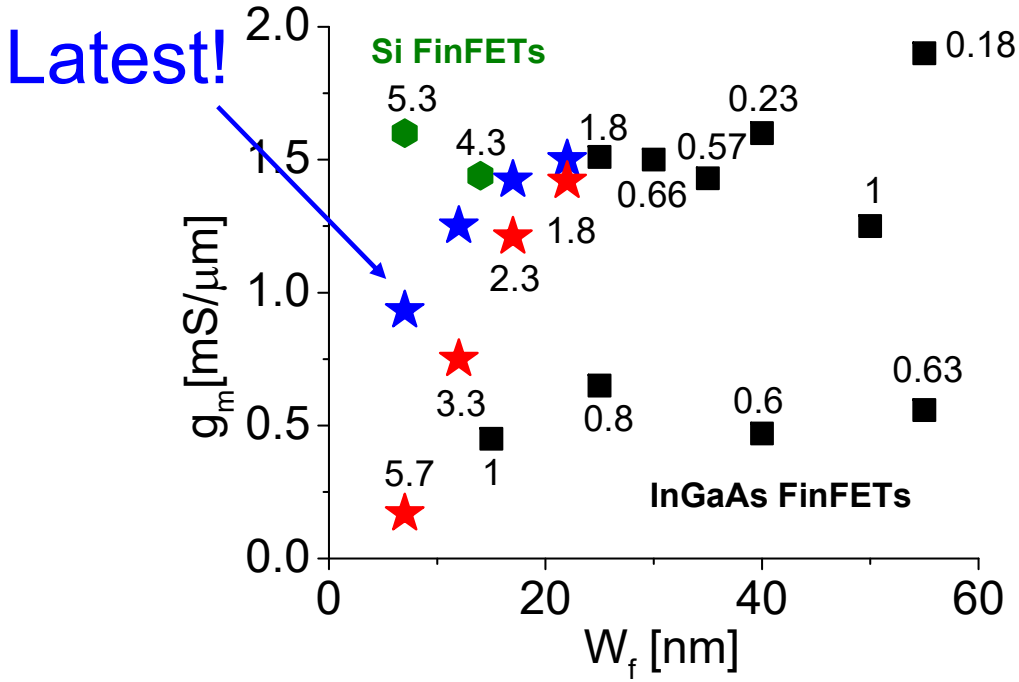
- First InGaAs FinFETs with W_f<10 nm
- Severe g_m degradation for thin W_f → sidewall roughness?

Latest results

- Scaled gate oxide: HfO_2 with EOT=0.6 nm
- Attention to line-edge roughness



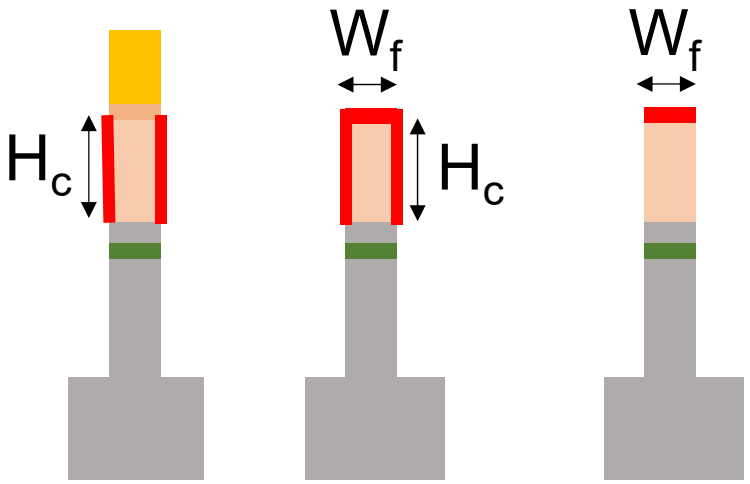
Vardi, submitted 2016



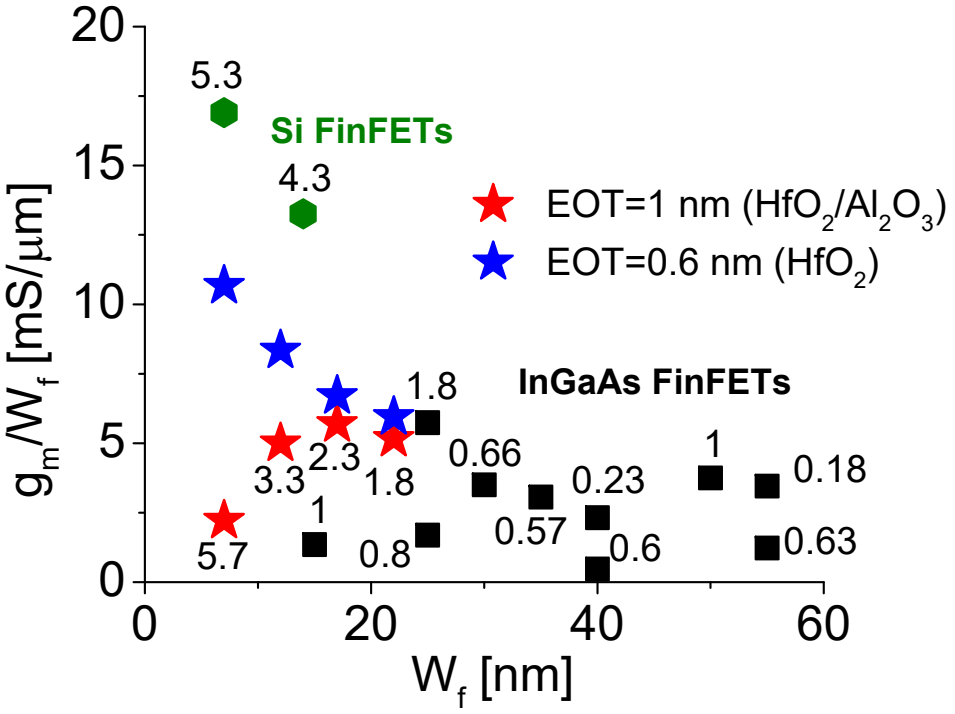
Record results for InGaAs FinFETs with $W_f < 25$ nm

InGaAs FinFETs: g_m benchmarking

g_m normalized by fin width (FOM for density):



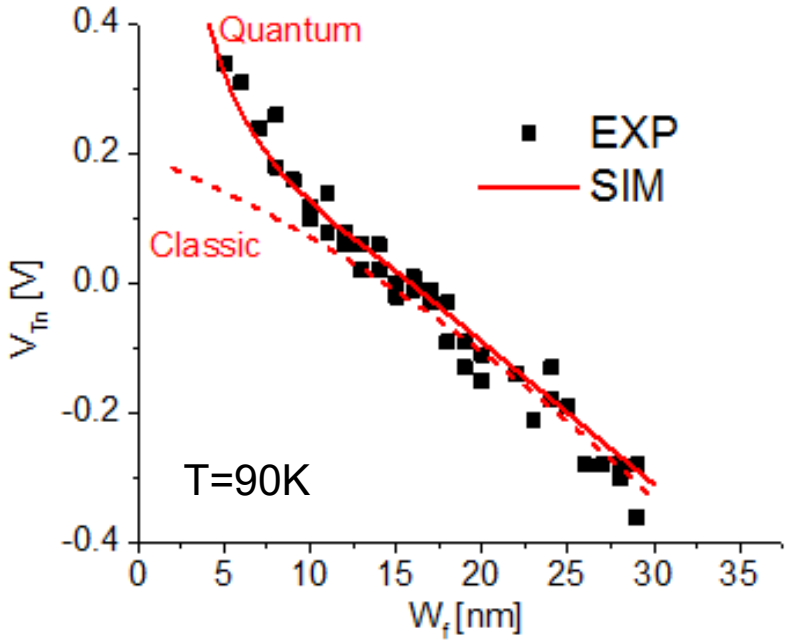
Vardi, submitted 2016

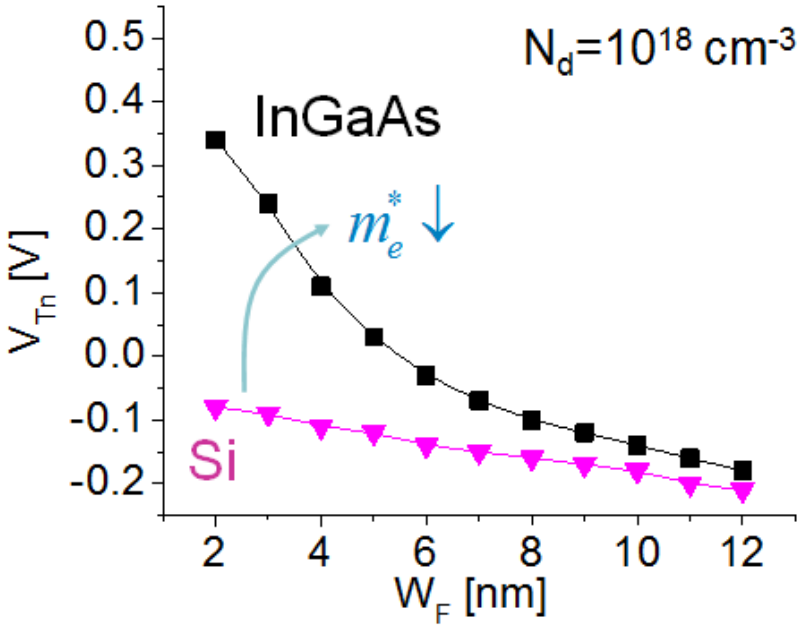


- Doubled g_m over earlier InGaAs FinFETs
- Still far below Si FinFETs → poor sidewall charge control

Impact of fin width on V_T

InGaAs doped-channel FinFETs: 50 nm thick, N_D~10^{18} cm^{-3}

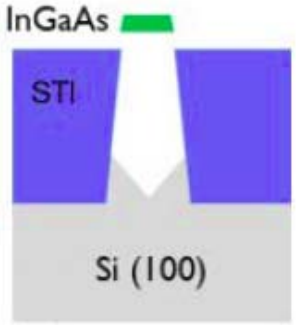


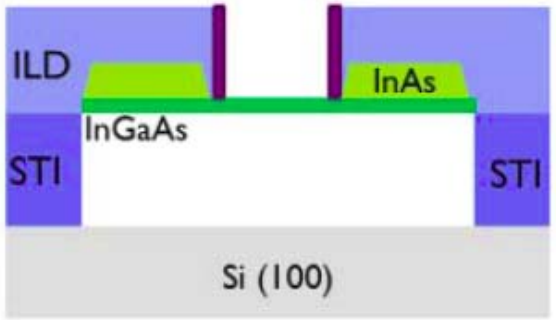


- Strong V_T sensitivity for W_f < 10 nm; much worse than Si
- Due to quantum effects

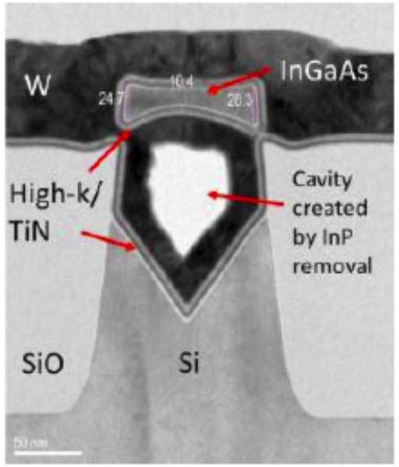
Vardi, IEDM 2015

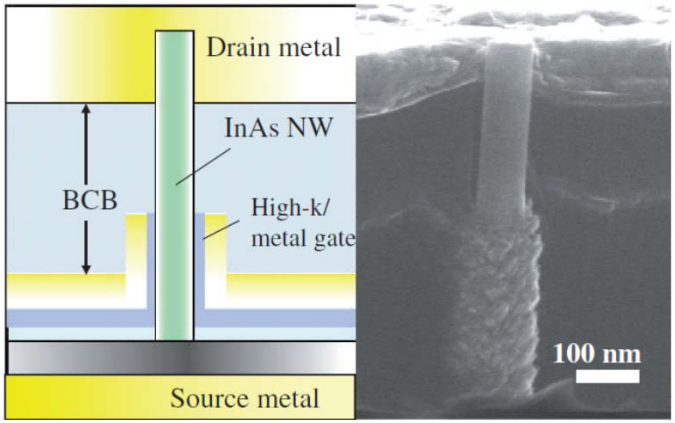
3. Nanowire InGaAs MOSFETs



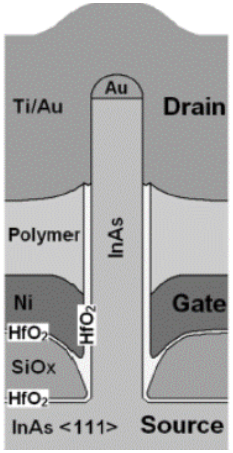


Waldron, EDL 2014

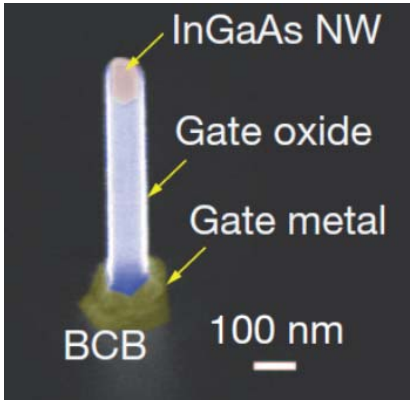




Tanaka, APEX 2010



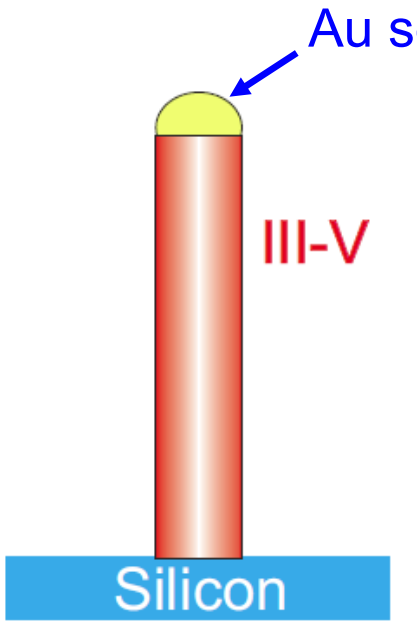
Persson, EDL 2012



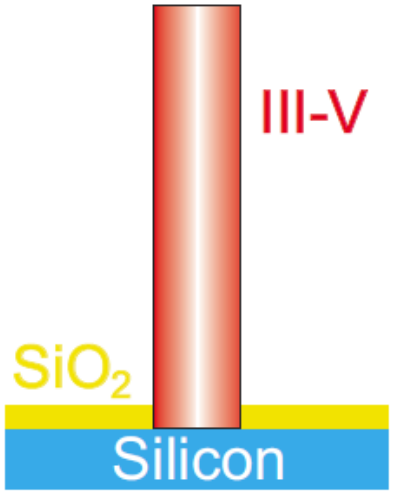
Tomioka, Nature 2012

- Nanowire MOSFET: ultimate scalable transistor
- Vertical NW: uncouples footprint scaling from L_g and L_c scaling

InGaAs Vertical Nanowires on Si by direct growth

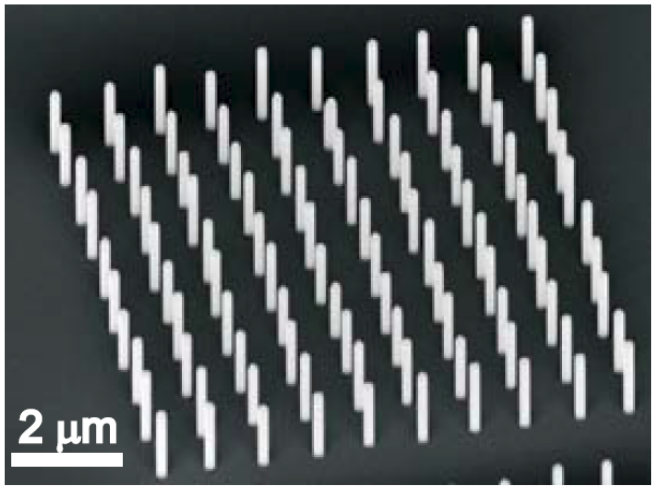


Vapor-Solid-Liquid (VLS) Technique

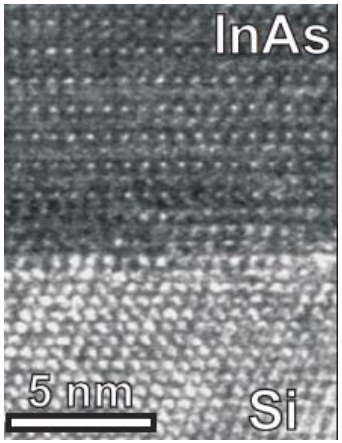


Selective-Area Epitaxy

Riel, MRS Bull 2014



InAs NWs on Si by SAE

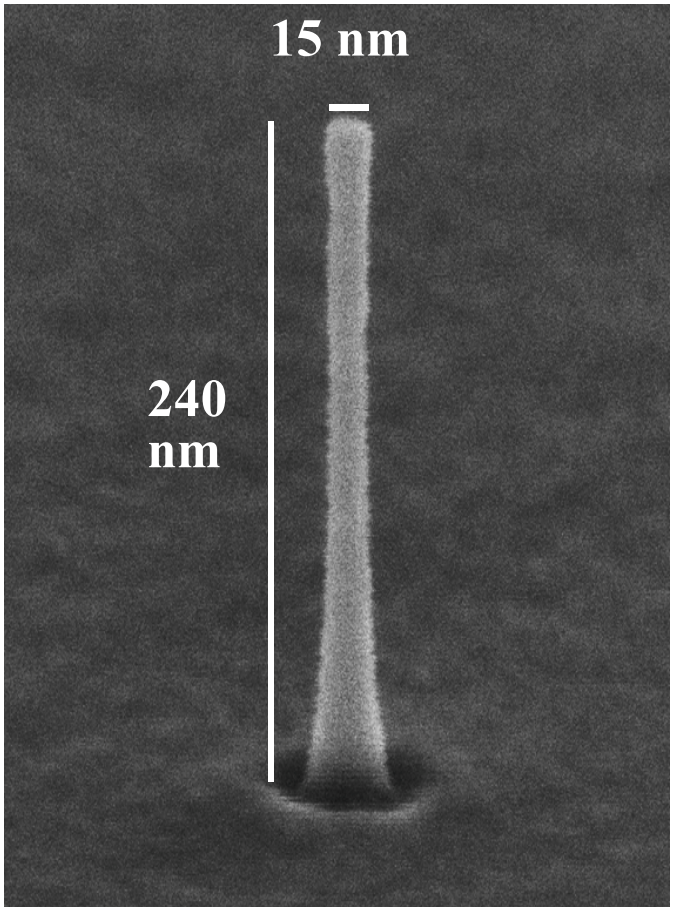


Björk, JCG 2012

InGaAs VNW MOSFETs by top-down approach @ MIT

Key enabling technologies:

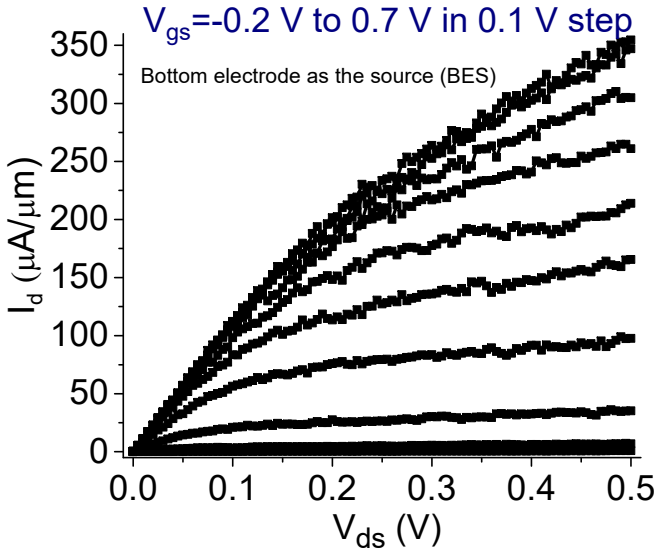
- RIE = $BCl_3/SiCl_4/Ar$ chemistry
- Digital Etch (DE) =
  - O_2 plasma oxidation
  - H_2SO_4 oxide removal

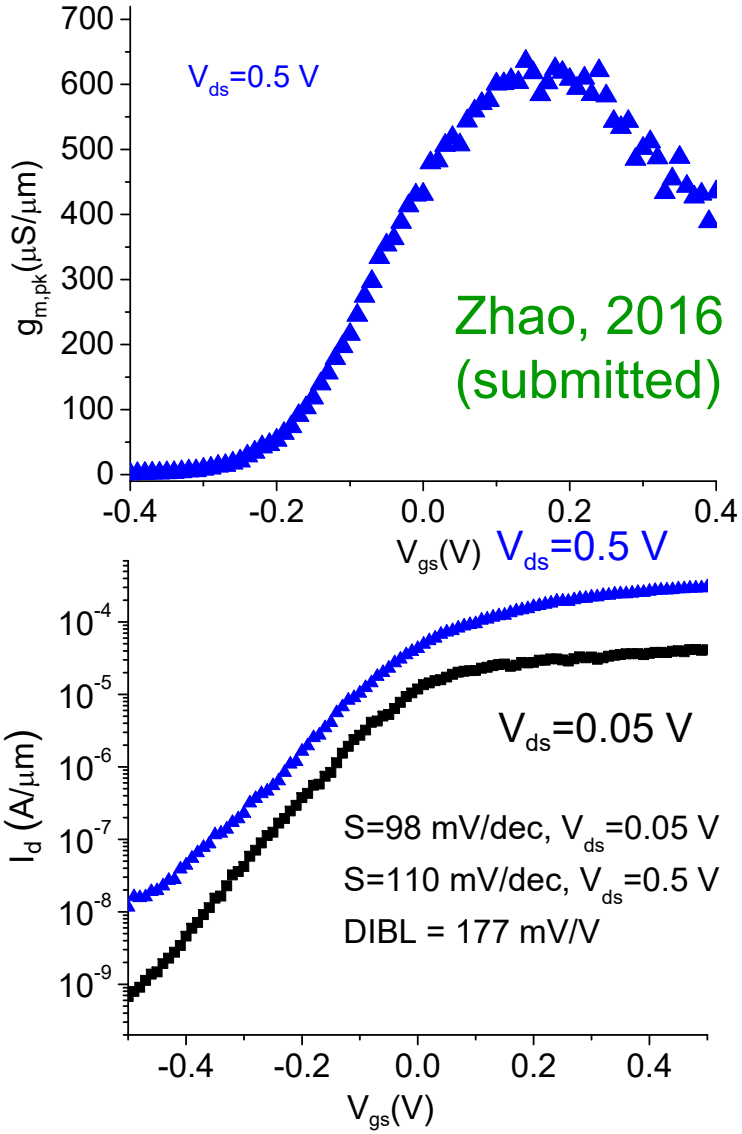


- Sub-20 nm NW diameter
- Aspect ratio > 10
- Smooth sidewalls

Zhao, EDL 2014

NW-MOSFET I-V characteristics: D=40 nm



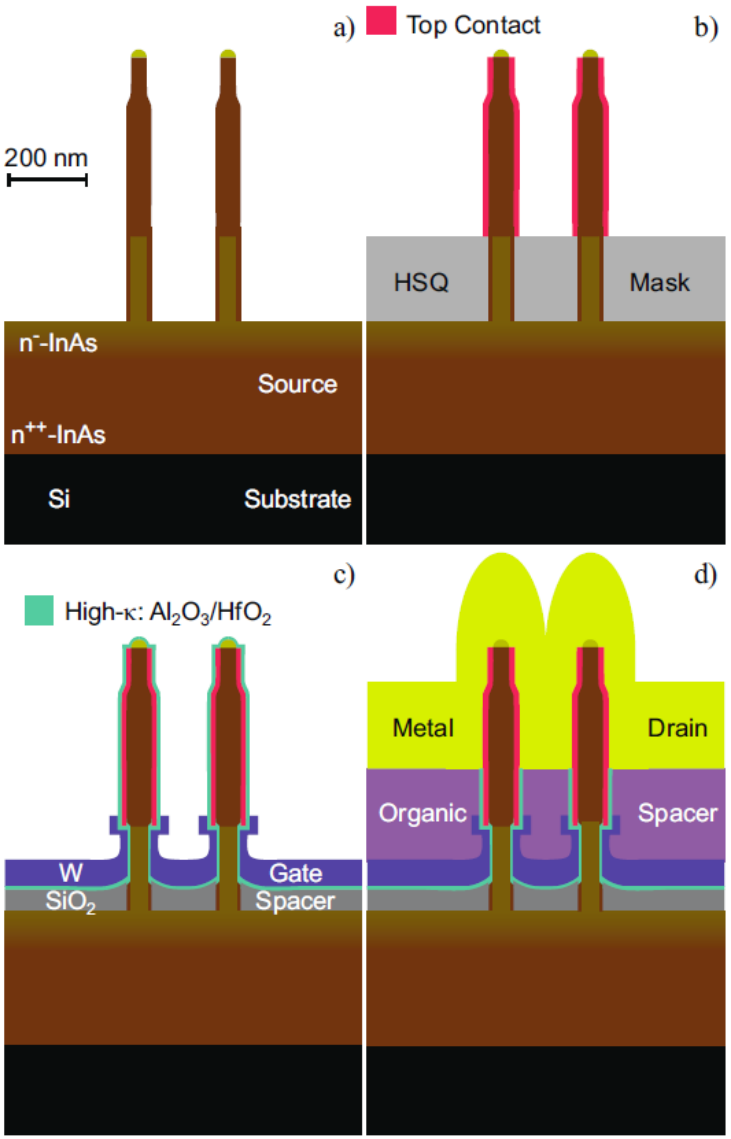


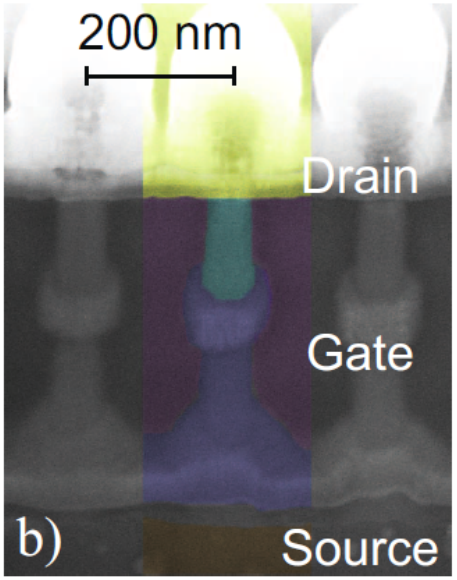
Single nanowire MOSFET:

- L_{ch}= 80 nm
- 3 nm Al_2O_3 (EOT = 1.5 nm)
- $g_{m,pk}$=620 μS/μm @ V_{DS}=0.5 V
- S_{sat}=110 mV/dec @ V_{DS}=0.5 V
- Approaches best bottom-up devices

[Berg, IEDM 2015]

Self-aligned Bottom-up InAs NW-MOSFETs



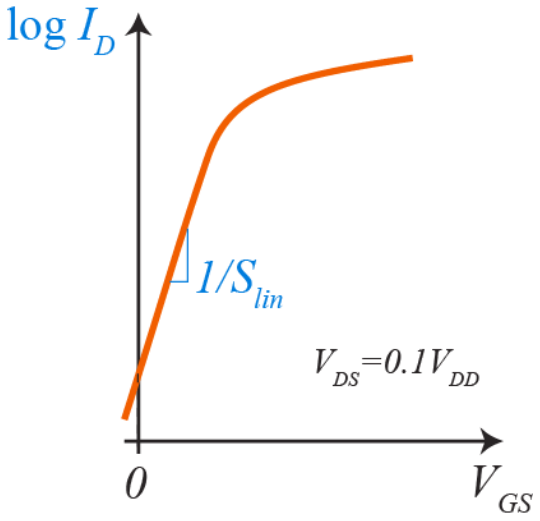


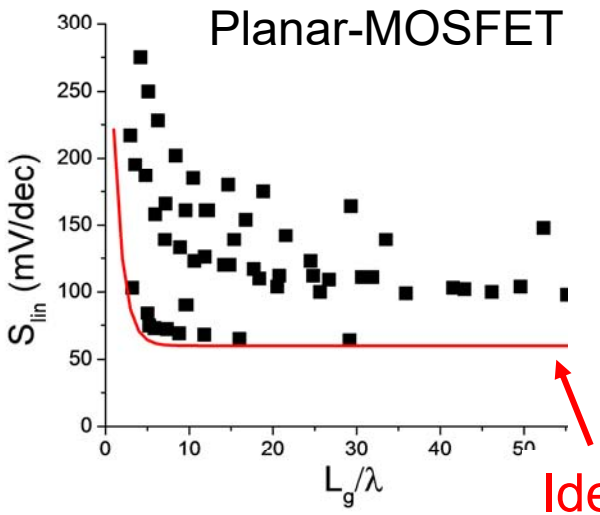
Berg, IEDM 2015

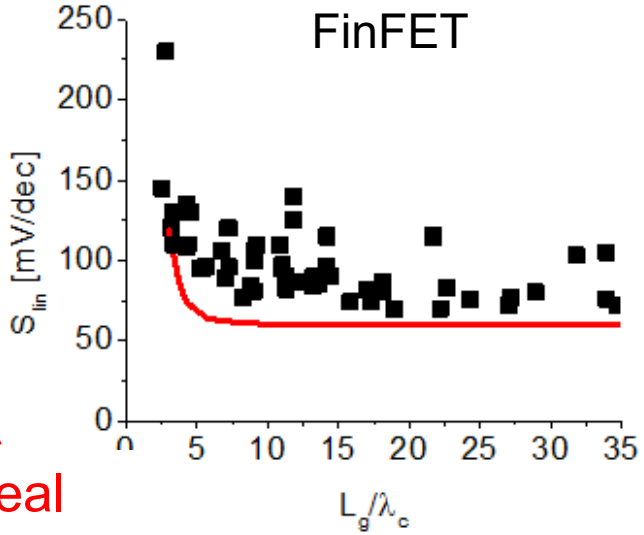
VNW MOSFET array:

- VLS growth
- D=28 nm
- L_{ch}= 190 nm
- $g_{m,pk}$=850 μS/μm @ V_{DS}=0.5 V
- S_{sat}=154 mV/dec @ V_{DS}=0.5 V

How are we doing in terms of short-channel effects?





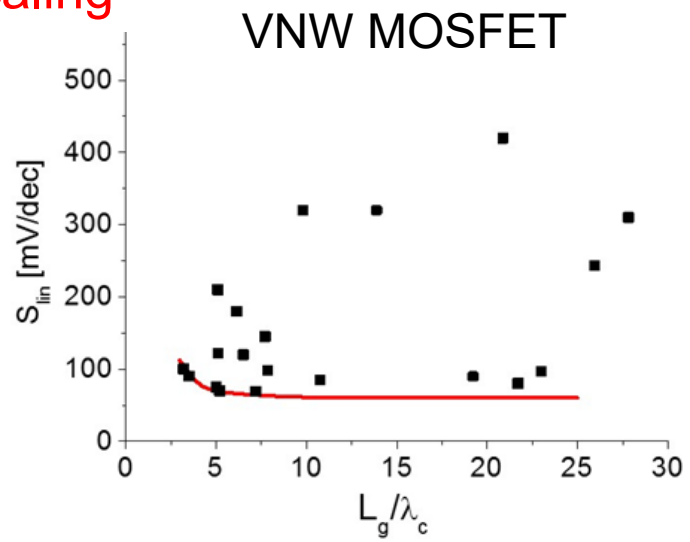


Ideal scaling

S_{lin}: linear subthreshold swing

L_g= gate length

λ_c= electrostatic scaling length: f(t_{ox}, t_{ch})

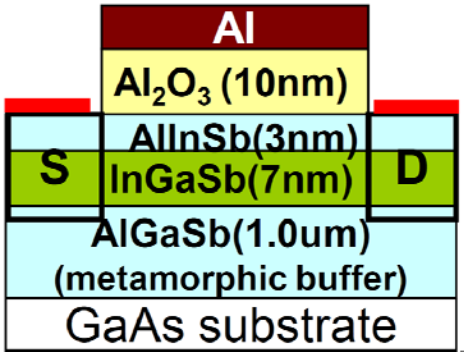


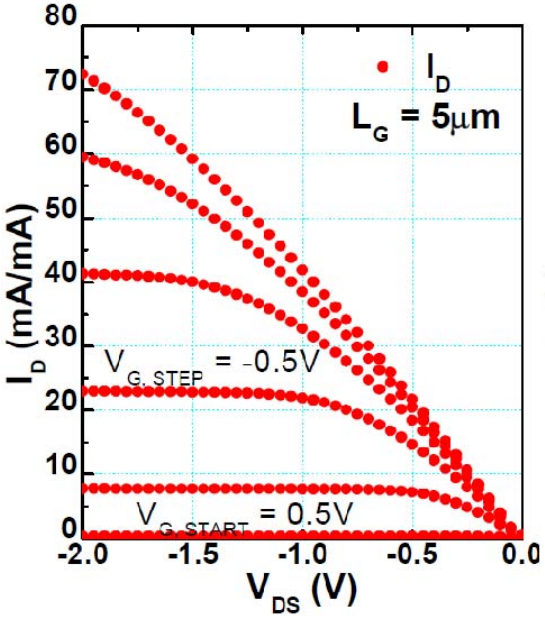
- Reasonable scaling behavior but…
- Excessive D_{it}

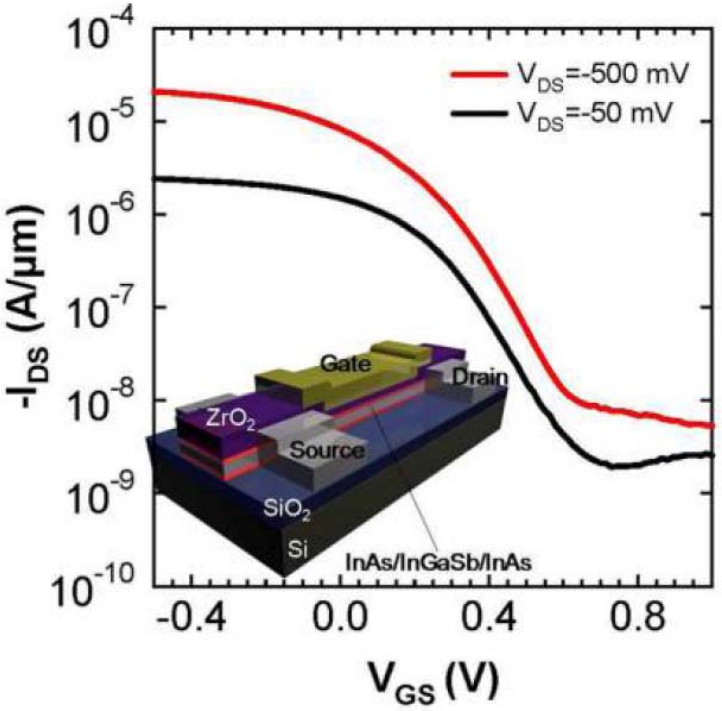
del Alamo, J-EDS 2016

4. InGaSb p–type MOSFETs

Planar InGaSb MOSFET demonstrations:







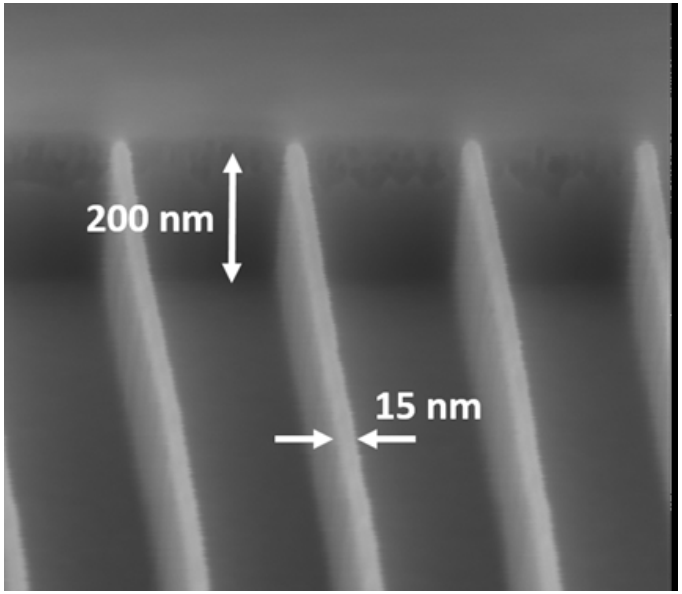
Nainani, IEDM 2010

Takei, Nano Lett. 2012

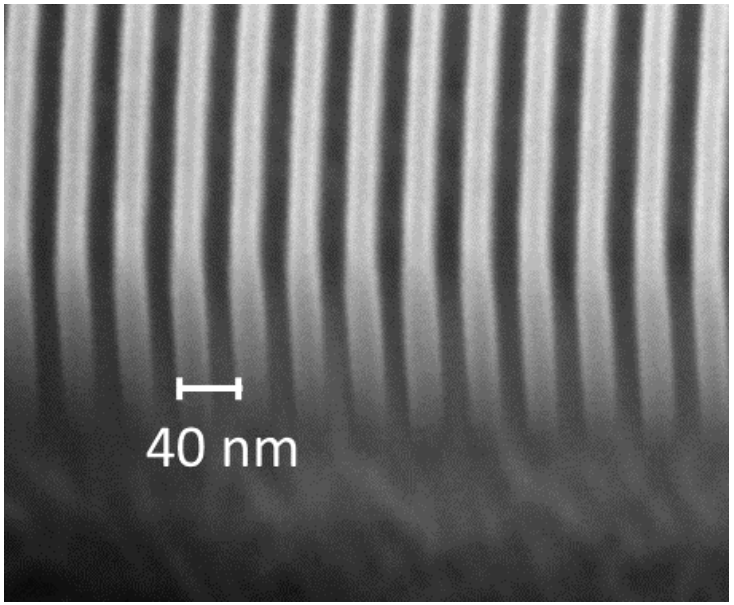
InGaSb p–type FinFETs @ MIT

Key enabling technology:

- BCl_3/N_2 RIE
- [digital etch under development]



15 nm fins, AR>13

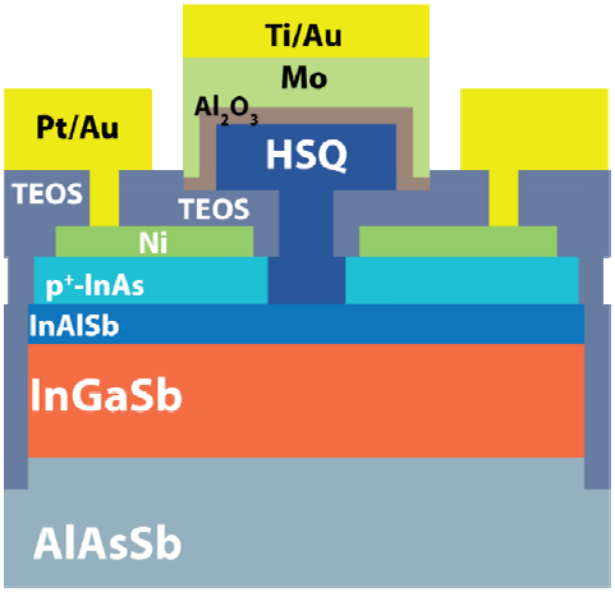


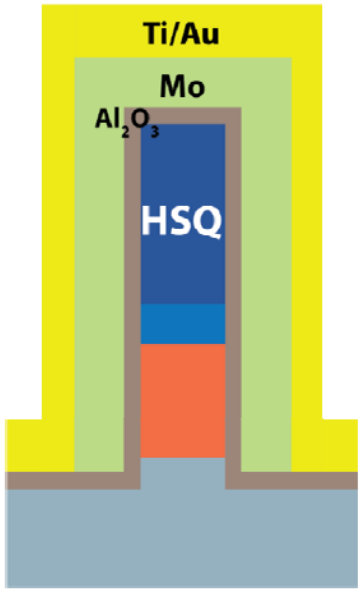
20 nm fins, 20 nm spacing

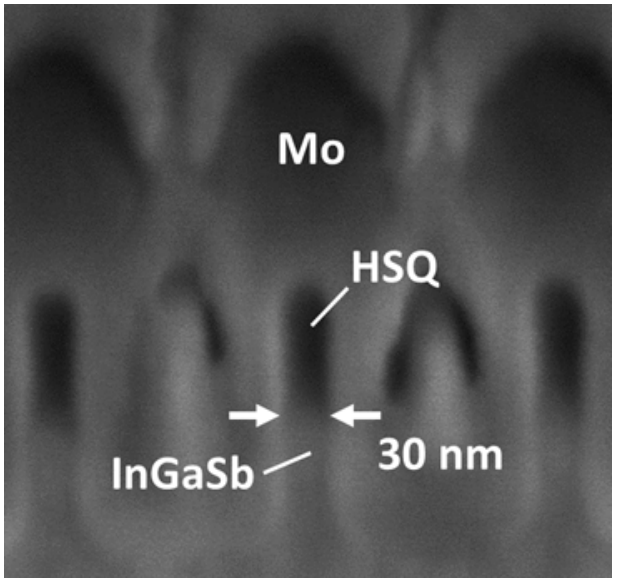
- Smallest W_f = 15 nm
- Aspect ratio >10
- Fin angle > 85°
- Dense fin patterns

Lu, IEDM 2015

InGaSb p-type FinFETs





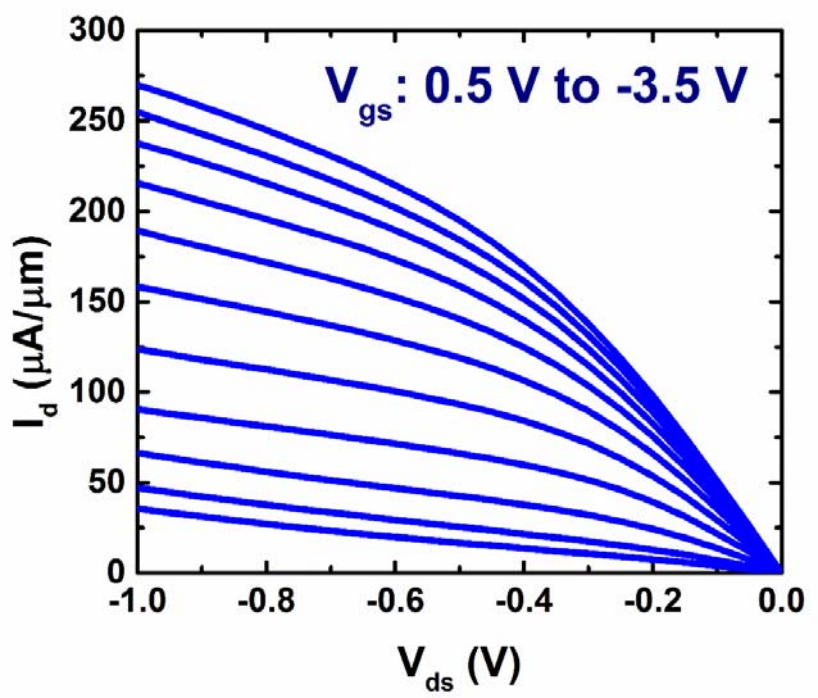


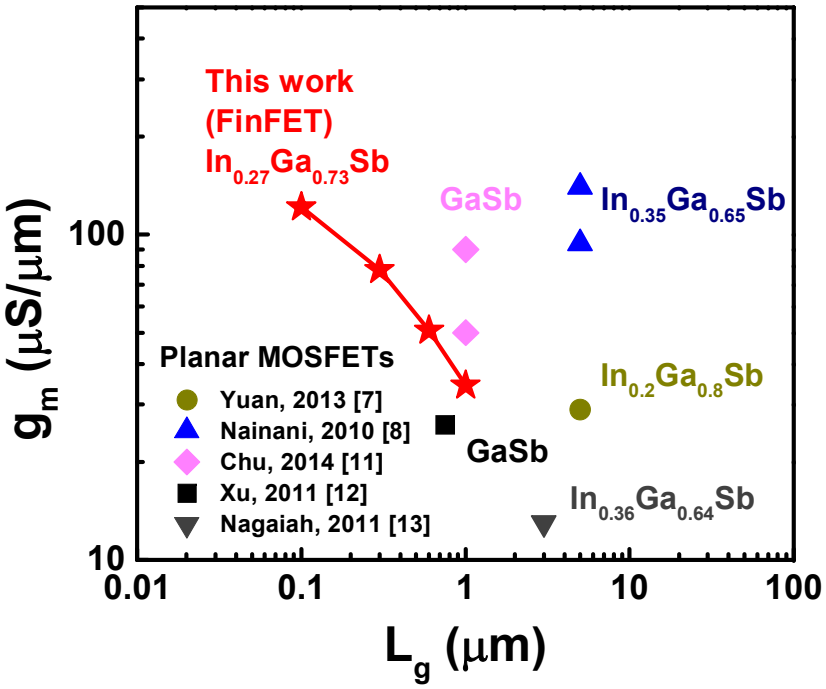
- Fin etch mask left in place → double-gate MOSFET
- Channel: 10 nm $In_{0.27}Ga_{0.73}Sb$ (compressively strained)
- Gate oxide: 4 nm Al_2O_3 (EOT=1.8 nm)

Lu, IEDM 2015

InGaSb FinFET I-V characteristics

- L_g = 100 nm, W_f = 30 nm (AR=0.33)
- Normalized by conducting gate periphery

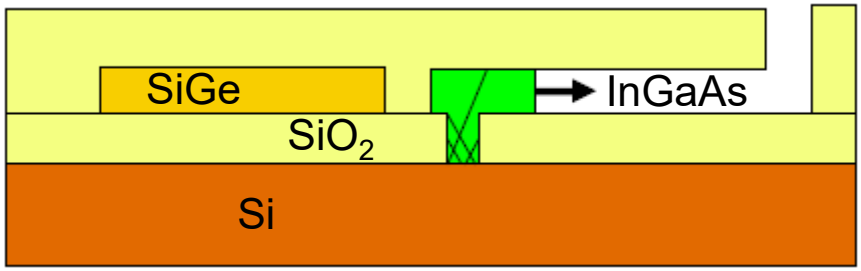




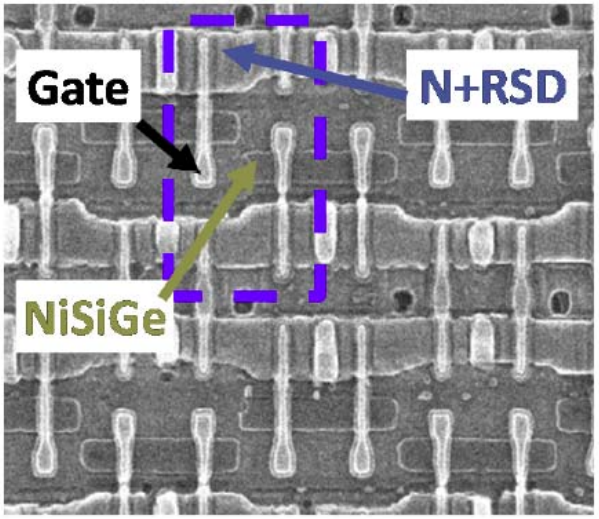
- First InGaSb FinFET
- Peak g_m approaches best InGaSb planar MOSFETs
- Poor turn off

Lu, IEDM 2015

Co-integration of SiGe p-MOSFETs and InGaAs MOSFETs on SOI



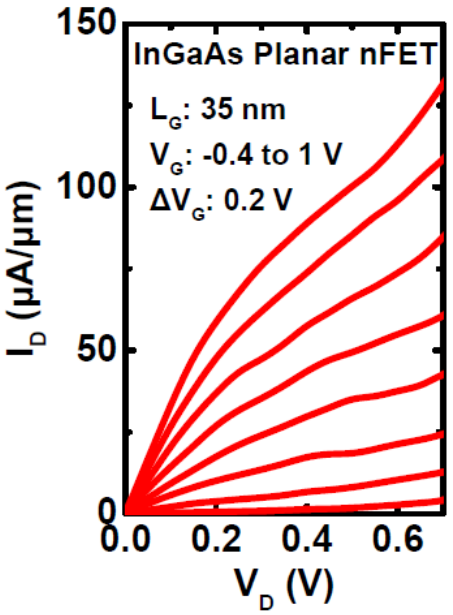
Confined Epitaxial Lateral Overgrowth



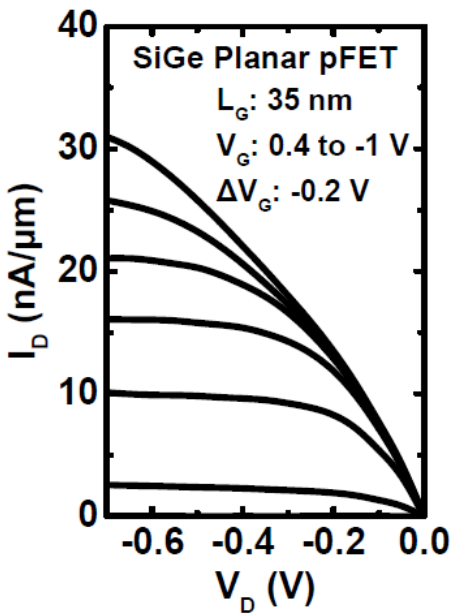
6T-SRAM

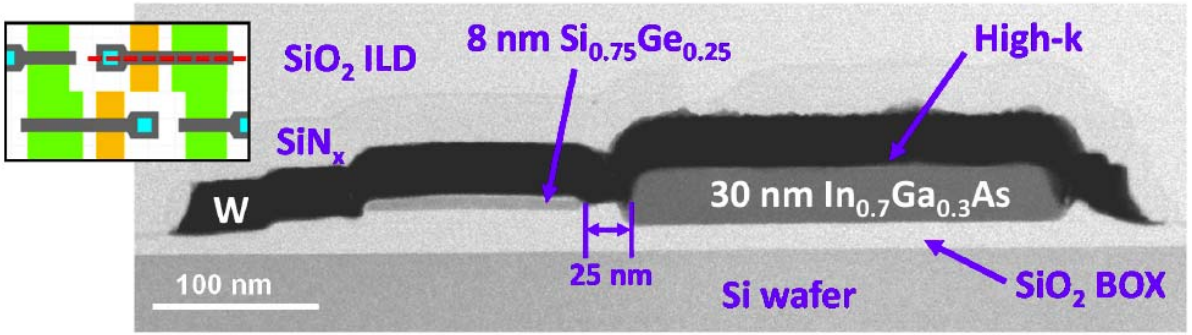
Czornomaz,
VLSI Tech 2016

InGaAs
n-MOSFET



SiGe
p-MOSFET





Conclusions

1. Great recent progress on planar, fin and nanowire InGaAs MOSFETs
2. Planar and multigate InGaAs MOSFETs exhibit nearly ideal electrostatic scaling behavior but poor D_{it}
3. Device performance still lacking for multigate designs
4. P-type InGaSb MOSFETs in their infancy
5. Many issues to work out:

   sub-10 nm fin/nanowire fabrication, self-aligned contacts, device asymmetry, introduction of mechanical stress, V_T control, sidewall roughness, device variability, BTBT and parasitic HBT gain, trapping, self-heating, reliability, NW survivability, co-integration on n- and p-channel devices on Si, …

A lot of work ahead but…
exciting future for III-V electronics